The Realization of an Area-Efficient CMOS Bandgap Reference Circuit with less than 1.25 V of Output Voltage Using a Fractional $V_{BE}$ Amplification Scheme

Hiroki SAKURAI, Student Member and Yasuhiro SUGIMOTO, Member

SUMMARY This paper describes a CMOS voltage reference circuit which occupies small die area and has less than 1.25 V of output voltage. The reference voltage is determined by a resistor ratio, and it is possible to set the reference voltage from zero to near the supply voltage with the same temperature independence as those of Widlar’s and Brokaw’s bandgap voltage references. The temperature-independent reference voltage is formed by adding two voltages: the amplified fractional $V_{BE}$ (base-to-emitter voltage) of a bipolar transistor with a negative TC (temperature coefficient) and the amplified $V_T$ (thermal voltage) with a positive TC. When a reference voltage smaller than 1.25 V is required, the voltage gain of the amplifier for $V_{BE}$ becomes less than one, and the voltage gain of the amplifier for $V_T$ becomes small. This enables the size of bipolar transistors for $V_T$ generation to be small. The proposed voltage reference circuit was implemented in a standard 0.35-um CMOS technology. A temperature-independent current source was also obtained from the same circuit. The results were a TC (temperature coefficient) of 46 ppm/$^\circ$C over 130$^\circ$C change, a line regulation of 2.2 mV/V for the 0.5 V reference voltage with 8.7 uA of current consumption in the voltage reference part, and a 6% change over 130$^\circ$C change for the 13 uA current source.

key words: Voltage reference, low reference voltage, small diode area, $V_{BE}$ amplification, CMOS

1. Introduction

As the supply voltage of LSIs has recently approached 1 V [1], a temperature- and supply-voltage-independent voltage reference of less than 1V has become necessary to supply a stable voltage to LSIs, for example, as can be seen in mobile communication equipment [2] where a buck DC-DC converter can supply this low voltage by down-converting the battery voltage without reducing power efficiency.

The temperature- and power-supply-independent voltage reference is formed utilizing bipolar technology by summing two voltages: the $V_{BE}$ with a negative TC and a multiple of $V_T$ with a positive TC [3]-[5]. As the TC of $V_{BE}$ is much larger than that of $V_T$, it is necessary for the $V_T$ to be multiplied by a large number. As a result, the reference voltage with zero TC becomes around 1.25 V. A reference voltage of less than 1.25 V can be obtained by reducing the 1.25 V with zero TC by using resistors [4]. However, this requires high performance bipolar transistors and is, therefore, not suitable to CMOS realization.

In order to realize the CMOS voltage reference with a reference voltage of less than 1.25 V with zero TC, a method of synthesizing current with a zero TC from two different currents with equal values of positive and negative TCs is used [6]-[8]. The synthesized current is applied to the output resistor and arbitrary output voltages such as 600 mV in [7] and 1.08 V in [8], respectively, are obtained. However, to obtain zero TC for the synthesized current, it was still necessary to multiply the current with positive TC by a large number. This made the size of the auxiliary substrate bipolar transistors that are available in conventional CMOS process excessively large.

In [9], the fractional $V_{BE}$ scheme to realize the low reference voltage such as 240 mV is introduced. As the absolute-value voltage change with temperature becomes small for a fractional $V_{BE}$ with a negative TC, a small voltage change with a positive TC can be compensated for, and a low stable reference voltage with zero TC obtained. However, multiplication of the $V_T$ by a large number is still necessary. In [10] this is realized with small size of auxiliary substrate bipolar transistors by cascading them and producing two currents with negative TC and positive TC. Those two TC values do not need to be the same in this case. Then, by using a differential op-amp, each of the two currents is converted to a voltage and added together to form the floating reference voltage with zero TC. However, cascading of auxiliary substrate bipolar transistors is the obstacle to obtain the low-voltage operation. They have not used the fractional $V_{BE}$ scheme for this purpose in order to reduce the bipolar transistor size. The power consumption of 2.2 mW is rather large.

The purpose of this paper is first to provide a CMOS voltage reference with less than 1 V of reference voltage and a constant current source with zero TC [11]. The second is to reduce the area for the auxiliary substrate bipolar transistors, and the third is to enable low voltage operation with low power consumption.
In Section 2, the prior technique to realize less-than-1.25 V reference voltage is reviewed. Section 3 introduces a circuit to obtain the fractional $V_{BE}$ separately from $V_T$ amplification. Section 4 describes the circuit structure of this voltage reference and analyzes power consumption and temperature characteristics. Section 5 shows the IC circuit designed to verify this concept, and Section 6 reports the evaluation results for the IC implementation. Section 7 concludes this paper.

2. Prior technique to realize the less-than-1.25 V reference voltage

2.1 Generating voltages with equal but opposite-sign TCs

We begin by re-visiting the basic concept of the bandgap voltage reference whose circuit is shown in Figure 1 [5]. The supply-voltage-independent characteristic is obtained when high-impedance elements such as current sources are used between the supply voltage and the voltage reference part. We consider only the temperature dependence of the voltage reference achieved by this circuit design.

The basic concept to obtain temperature independence is to add two voltages, one with negative and one with positive TC. The goal is to obtain two voltages with equal but opposite-sign TCs. In Figure 1, $V_{BE}$ is the voltage across the diode D and has a negative TC of approximately -2 mV/°C at room temperature. This diode is commonly constructed by using an auxiliary substrate bipolar transistor in the standard CMOS process. By contrast, the thermal voltage $V_T$, which is obtained by using two auxiliary substrate bipolar transistors in diode connection and a resistor, has a positive TC of approximately +0.086 mV/°C at room temperature.

As the positive TC is about 23 times smaller than the negative TC, it is necessary for the positive TC to be amplified by A ($A=23$) to match the negative TC. This means that the DC voltage associated with the positive TC becomes nearly 600 mV at room temperature. As $V_{BE}$ is about 650 mV, the summation of these two voltages becomes approximately 1.25 V. The TCs of these voltages are of same value but opposite in sign, and the resultant reference voltage has zero TC.

2.2 The synthesizing current scheme

The voltage reference in [6] realized this TC cancellation in its current form. Figure 2 shows the circuit. The role of the operational amplifier is to equalize voltages at the positive and negative input terminals. The voltage across the diode D1 and the voltage across the resistor R1 plus that across the diode D2 become equal. Taking the offset voltage $V_{off}$ of the operational amplifier (op-amp) into account, the following equation holds.

$$V_{BED1} + V_{off} = i_{A1}R_1 + V_{BED2} \quad (1)$$

Provided that D2 is an N-multiple of D1, and that $i_A = i_B$ because they are simply the currents from current mirrors, $i_{A1}$ becomes

$$i_{A1} = \frac{kT}{q} \ln N + \frac{V_{off}}{R_1} \quad (2)$$

where $k$ is Boltzmann’s constant ($1.38 \times 10^{-23}$ J/K), $q$ is the electronic charge ($1.62 \times 10^{-19}$ C), and $T$ is the absolute temperature. The current $i_{A1}$ is proportional to the thermal voltage $V_T$ ($kT/q$: approximately 26 mV at room temperature), and has positive TC if we assume the offset voltage $V_{off}$ of the op-amp is constant. As the voltage at terminal B is the voltage across the diode D1 and it is $V_{BE}$, the voltage at terminal A can be expressed as $V_{BED1} + V_{off}$ in terms of the voltage at terminal B. Then, the current $i_{A2}$ in the resistor R2 becomes

$$i_{A2} = \frac{V_{BED1} + V_{off}}{R_2} \quad (3)$$

Current $i_A$, which is the sum of $i_{A1}$ and $i_{A2}$, therefore...
becomes
\[
i_A = \frac{V_{BED1}}{R_2} + \frac{V_T}{R_1} \ln N + \left( \frac{1}{R_1} + \frac{1}{R_2} \right) V_{off} \quad (4)
\]

Current \(i_A\) is the current of \(M_{p2}\). As \(M_{p1}\), \(M_{p2}\), and \(M_{p3}\) form a current mirror as seen in Figure 2, we can assume \(i_A = i_B = i_C\). As a result, the \(V_{REF}\), which is the voltage across \(R_3\), becomes
\[
V_{REF} = \frac{R_3}{R_2} \left[ \frac{V_{BED1}}{R_2} + \left( \frac{R_2}{R_1} \right) V_T \ln N \right]
+ \left( 1 + \frac{R_2}{R_1} \right) V_{off} \quad (5)
\]

It is understood from equation (5) that it is necessary to equate the absolute value of TCs between \(V_{BE}\) and the voltage \((R_2/R_1)V_T \ln N\). The TC of \(V_{BE}\) is negative and the TC of the voltage \((R_2/R_1)V_T \ln N\) is positive. Note, however, that the TC of \(V_{BE}\) is about 23 times larger than that of \(V_T\). This leads to
\[
\frac{R_2}{R_1} \ln N \approx 23 \quad (6)
\]

The relationship in equation (6) holds for the circuits in both [6] and [7]. The circuit in [8] contains the term \((R_2/R_1)V_T \ln N\). However, the voltage with a negative TC corresponding to \(V_{BE}\) in equation (5) is replaced by a term corresponding to the threshold voltage of a PMOS transistor, and the value \((R_2/R_1)\ln N\) is different.

2.3 Example calculation

As \(\ln N = 5\) or \(\ln N = 4\) implies that \(N\) needs to be 148 or 54, respectively, we need to have a large number of diodes in parallel for D2 in Figure 2. When the \(N\) value is large, however, \(V_T \ln N\) becomes large and it is necessary for \(R_1\) to increase its value in order to minimize power consumption as can be seen in equation (2). To preserve the relationship shown in equation (6), \(R_2\) becomes large at the same time. Equation (5) indicates that the influence of the offset voltage of the op-amp is determined by \(R_2/R_1\) and is not changed by this modification. If we ignore offset voltage of the op-amp, then the value in the large braces in equation (5) becomes equal to the voltages of Widlar’s and Brokaw’s voltage references, those of which are equal and are 1.25 V. As the equation in Widlar’s circuit exactly agrees with the part in the large braces in equation (5), it is convenient to compare the characteristics with the low-voltage operational MOS voltage references in which auxiliary substrate bipolar transistor is not cascaded.

However, Brokaw’s circuit now becomes common to use in bipolar circuits because of its small resistor ratio or small transistor size ratio. In Brokaw’s circuit, the term \(R_2/R_1\) in equation (5) should be replaced by \(2R_2'/R_1\), however, the terms are equal in value.

Now, the currents \(i_A\), \(i_B\), and \(i_C\) all become approximately \(1.25/R_2\). This means that the current consumption is solely determined by the \(R_2\) value. Therefore, it is better in this circuit to increase the \(R_1\) and \(R_2\) values. The chip area, however, becomes large because of large values of \(N\), \(R_1\) and \(R_2\).

3. A method of independently producing the fractional \(V_{BE}\) voltage

It is evident from equation (6) that the \(N\) value must be very large to obtain a voltage reference with zero TC. Suppose that we could reduce 23 in the right-hand side of equation (6) to one-third of this value. If \(R_2/R_1\) does not change, then the \(\ln N\) value becomes 1/3. This means that the \(N\) value is decreased by \(1/e^3\) where \(e\) is the exponential value. To realize this, we can not increase the \(R_2/R_1\) value by 3. The simplest way is to reduce \(V_{BE}\) to one-third of its present value. If \(V_{BE}\) is divided by 3, then \((R_2/R_1)\ln N\) also becomes 1/3, indicating that the \(N\) value is decreased by \(1/e^3\). Note that the realization of this fractional \(V_{BE}\) should be achieved separately from the \(V_T\) generation. Otherwise, it leads to the same result as that of equation (6).

In order to produce a fractional \(V_{BE}\) separately, we use the circuit shown in Figure 3. The similar circuit structure is seen in [8] and [10]. However, they are not intended to reduce the size of the auxiliary substrate bipolar transistor. The output current of the circuit in [8] should have a negative TC with its absolute value equal to that of a positive TC which is supplied from the other part. The resistor values in the circuit should be adjusted for this purpose. The circuit in Figure 3 is simply a \(V_{BE}\) amplifier whose voltage gain is \(R_3/(L \times R_2)\), where L is the current-mirror ratio between J1 and J2 and is chosen to be one in this design. To maintain the linearity of the \(V_{BE}\) amplifier, op-amp A2 and Mn1 are used to exactly equate voltages between terminals B and C in Figure 3. This is different from the circuit in [10]. Linearity of the circuit in [10] is reduced due to the lack of an op-amp.
4. **A circuit to generate a less-than-1.25 V reference voltage with zero TC**

4.1 **The voltage reference circuit**

We now know a method to produce a fractional $V_{BE}$. Next, a fractional $V_{BE}$ and the multiple of the thermal voltage $V_T$ should be added to form the $V_{REF}$ of less than 1.25 V. Note that only the small voltage proportional to the thermal voltage $V_T$ is needed to cancel the TC of a fractional $V_{BE}$. The circuit shown in Figure 4 achieves this. By introducing $R_3$ in series with $R_3$ as shown in Figure 4, we can avoid duplicating $R_3$ and obtain the voltage reference related to ground potential. The circuit, consisting of diodes D1 and D2, op-amp A1, resistor R1 and transistors Mp1, Mp2 and Mp3, produces current $i_C$ given by

$$i_C = \frac{kT}{q} \ln N + V_{off1}$$

(7)

Here, assumptions are made that $i_A=i_B=i_C$ and that the voltage difference between inputs of op-amp A1 is zero. As the current $i_C$ flows in resistors R3 and R4, the voltage $V_P$, which is equal to $I_C \times (R_3 + R_4)$ and has a positive TC, becomes

$$V_P = \frac{R_3 + R_4}{R_1} \left( \frac{kT}{q} \ln N + V_{off1} \right)$$

(8)

The voltage $V_N$ across R3, which is produced by the current $i_N$ is calculated as

$$V_N = \frac{R_3}{L \times R_2} (V_{BED1} - V_{off2})$$

(9)

Of course, $V_N$ has a negative TC. The resultant voltage reference $V_{REF}$ is obtained by the addition of equations (8) and (9); hence,

$$V_{REF} = V_P + V_N$$

$$= \frac{R_3}{L \times R_2} V_{BED1} + \frac{R_3 + R_4}{R_1} V_T \ln N$$

$$+ \frac{R_3 + R_4}{R_1} V_{off1} - \frac{R_3}{L \times R_2} V_{off2}$$

$$= \frac{R_3}{L \times R_2} \left[ V_{BED1} + \frac{R_2}{R_1} (1 + \frac{R_4}{R_3}) V_T \ln N \right]$$

$$+ \frac{L \times R_2}{R_1} \left( 1 + \frac{R_4}{R_3} \right) [V_{off1} + |V_{off2}|]$$

(10)

Note that we cannot tell whether the offset voltage is positive or negative, and the absolute value is used. From equation (10), we obtain for a $V_{REF}$ with zero TC

$$\frac{L \times R_2}{R_1} \left( 1 + \frac{R_4}{R_3} \right) \ln N \approx 23$$

(11)

Equation (11) clearly shows that $\ln N$ can be reduced by the factor of $L \left( 1 + \frac{R_4}{R_3} \right)$ compared with equation (6). As for the offset voltages of the op-amps appearing in equation (10), $V_{off1}$ is multiplied by the factor $\left( L \times R_2/R_1 \right) \left( 1 + \frac{R_4}{R_3} \right)$ while $V_{off2}$ appears as it is. Usually, in the case when the reference voltage is below 1 V and L equals 1, the relation $R_2 > R_3 > R_1$, and $R_4 \approx R_3$ hold. Therefore, the influence of $V_{off1}$ is much greater than that of $V_{off2}$. The influence of $V_{off1}$ in Figure 4 might become greater than that of $V_{off2}$ in Figure 2 because the factor $\left( L \times R_2/R_1 \right) \left( 1 + \frac{R_4}{R_3} \right)$ in equation (10) is larger than the factor $\left( 1 + \frac{R_4}{R_3} \right)$ in equation (5). The above discussion tells us that we must be careful to design op-amp A1 in such a way that it does not have a large offset voltage; the offset voltage of A2 is inconsequential.

4.2 **Power consumption and temperature dependence**

The total current of the circuit in Figure 2 excluding currents of the op-amp is $3(i_{A1} + i_{A2})$ when $i_{A1}=i_{B1}$ and $i_{A2}=i_{B2}$ are assumed, while the total current of the circuit in Figure 4 excluding currents of op-amps is $3i_{A1} + 2i_N$ provided that $i_{A1}=i_{B1}$ and $L=1$. When the same voltage is chosen for $V_{REF}$ in both circuits, the ratio $R_3/R_2$ in equations (5) and (10) becomes equal. Suppose that the R1, R2, and R3 values in Figure 2 and 4 are each identical. As the area factor N of diodes D1 and D2 in Figure 4 becomes smaller than that in Figure 2, current $i_A$ in Figure 4 becomes smaller than current $i_{A1}$ in Figure 2. In theory, the current consumption of the circuit in Figure 4 becomes smaller than that of the circuit in Figure 2 under these conditions. However, R1 might be increased to decrease the total current in Figure 2. As the circuit in Figure 4 has an additional resistor R4 and an op-amp A2, the comparison of current consumption and total resistor values becomes complex. It is always hard to tell which method is better until the final circuit design is obtained.
The temperature dependence of the circuit in Figure 4 does not differ from those of Widlar’s and Brokaw’s bandgap voltage references because the concept contained in both equations (5) and (10) is the same, namely, the cancellation of TCs between \( V_{BE} \) and \( V_T \). The \( V_{BE} \) voltage of a bipolar transistor is known to be expressed as [5]

\[
V_{BE}(T) = V_{G0} - V_T \ln \frac{T}{T_0} + \alpha \ln T - \ln E \tag{12}
\]

where \( V_{G0} \) is the extrapolated silicon band-gap voltage to \( 0^\circ \text{K} \), \( \gamma = (4 - n) \), \( n \) is the TC of the electron and/or hole mobility, \( \alpha \) is the TC of the current which flows through a bipolar transistor, and \( E \) and \( G \) are constant.

We substitute equation (12) into equation (10) and take the derivative with respect to temperature, that is, \( dV_{BE}/dT \). We further choose \( (dV_{REF}/dT) \) \( T_0 \) to be zero in order for the \( V_{REF} \) to have zero TC at \( T = T_0 \). This leads to

\[
\frac{R_3 + R_4}{R_1} \ln N + \frac{R_3}{L \times R_2} \ln E \tag{13}
\]

By using equation (13), equation (10) reduces to

\[
V_{REF} = \frac{R_3}{L \times R_2} \left[ V_{G0} + V_T \left\{ (\gamma - \alpha) \left( 1 + \ln \frac{T_0}{T} \right) \right\} + V_{off} \left\{ 1 + \frac{L \times R_2}{R_1} \left( 1 + \frac{R_4}{R_3} \right) \right\} \right] \tag{14}
\]

where \( V_{off1} \) and \( V_{off2} \) in equation (10) are set equal to \( V_{off} \). Equation (14) indicates that the output voltage is rather arbitrarily determined by the resistor ratio \( (R_3/R_2) \) together with current mirror-ratio \( L \), and it ranges from ground to near the supply voltage. The first two terms in the brackets in equation (14) agree with those appearing in [5]; therefore, the same temperature dependence as for the bipolar bandgap voltage reference is expected. The above discussion describing the \( V_{REF} \) temperature dependence is also applicable to equation (5) and to the circuit in Figure 2, and the same results in equation (14) are obtained.

Equation (13) indicates that the condition to realize zero TC at temperature \( T_0 \) is adjusted by using the resistor \( R_4 \) independently of \( R_1 \), \( R_2 \) and \( R_3 \). It is apparent, in the case of equation (5) and the circuit in Figure 2, that we are obliged to change the \( R_1 \) value. It is very sensitive and difficult to adjust by small amounts because the ratio \( R_2/R_1 \) changes rapidly.

5. IC circuit design

5.1 Voltage circuit design

Figure 5 shows the design for fabrication using the 0.35 \( \mu \text{m} \) CMOS devices. Functions such as a temperature-independent constant current source and start-up circuitry has been added to the circuit of Figure 4. Diodes D1 and D2 appearing in Figure 5 consist of substrate pnp transistors, whose collectors are automatically tied to the ground terminal. The \( N \) and \( L \) values are set at 4 and 1, respectively. From the discussion of equation (11), an \( N \) value of 4 requires

\[
(R_2/R_1) \left\{ 1 + (R_4/R_3) \right\} \approx 16 \tag{15}
\]

We chose \( R_1 = 100 \, \text{k}\Omega \), \( R_2 = 800 \, \text{k}\Omega \), \( R_3 = 340 \, \text{k}\Omega \), and \( R_4 = 350 \, \text{k}\Omega \). The area and matching required for them were considered to be critical in this design. We used 20 \( \mu \text{m} \) resistor width to obtain good matching of the resistor ratios. The resistor width in actual production chips is usually 5 or 6 \( \mu \text{m} \), and the area for resistors is expected to become approximately 1/16 of this design.

The current consumption excluding the constant current source generation and start-up circuits is 8.7 \( \mu \text{A} \). Out of this 8.7 \( \mu \text{A} \), op-amp A1 uses 4 \( \mu \text{A} \) and op-amp A2 uses 2.1 \( \mu \text{A} \).

Degeneration resistors MJR1, MJR2, MpR1, MpR2, and MpR3 are used together with the PMOS current sources MJ1, MJ2, M1p, M2p, and M3p, respectively, to increase the output impedance of each current source so as to lessen the influence of supply voltage changes. Op-amp A1 has differential PMOS source followers at inputs followed by an NMOS differential amplifier with cascode connection of transistors to increase the open loop gain while operational amplifier A2 is of the simple PMOS input differential amplifier. The size of the PMOS source followers and input transistors of an NMOS differential amplifier of op-amp A1 are chosen large in order to reduce the input offset voltage.

5.2 Constant current source

The concept used to obtain the constant current source is the cancellation of resistor TC. In Figure 5, the op-amp A2 enables the source voltage of MIn1 to be equal to the voltage at A2’s positive input terminal; that is, D. Suppose this voltage is constant; then, the current flowing through R6 changes as temperature changes, because the TC of R6 is approximately -2600 ppm/°C. This means the voltage at terminal D should change by approximately -2600 ppm/°C to maintain a constant current. This is done by placing R5 in between terminals B and D. The effect of insertion of R5 is minimal in terms of mismatch of source-to-drain voltages of M1p and M2p because the impedance at terminal D is high due to the use of degeneration resistors MpR1 and MpR2 and because the value of R5 is small. Ignoring the offset voltage of the op-amp A1 and using equation (2), the voltage across R5 (\( V_{R5} \)) becomes,

\[
V_{R5} = i_B \times R_5 = i_A \times R_5 = \frac{R_5}{R_1} V_T \ln N \tag{16}
\]

where \( N \) is 4. Therefore \( V_{R5} \) has a positive TC whose
value is adjustable by changing the value of \( R_5 \). This positive TC doesn’t suffer from the resistors’ negative TC because \( V_{R_5} \) is determined by the ratio between \( R_5 \) and \( R_1 \) times \( V_T \ln N \). On the other hand, the voltage across \( D_1 \) has a negative TC, approximately -3000 ppm/°C. The series connection of these two voltages realizes an intermediate TC value for the voltage at terminal D. When \( R_5 \) is chosen 235 kΩ, the TC of \( V_{R_5} \) becomes +400 ppm/°C and the TC of voltage at terminal D becomes -2600 ppm/°C. As \( R_6 \) has a TC of -2600 ppm/°C, both TCs are cancel out, therefore, the current that flows in \( M_{In1} \) becomes independent of temperature change, and is distributed to other circuits through \( M_{In2} \) and the associated current-mirror circuits.

5.3 Start-up circuit

Special start-up circuitry is required for circuits having supply-voltage-independent characteristics. \( M_{sp1}, M_{sp2}, M_{sn1}, M_{sn2}, M_{sn3}, \) and \( R_7 \) in Figure 5 comprise the start-up circuit. When the supply voltage begins to increase in the start-up interval, the input voltage of the inverter which is formed by \( M_{sn1} \) and \( M_{sp1} \) is low; therefore, the output voltage of the inverter becomes high. This enables \( M_{sn2} \) and \( M_{sn3} \) to draw currents from the PMOS current sources in order to activate them. As the supply voltage rises, the output voltage of the inverter falls, and \( M_{sn2} \) and \( M_{sn3} \) are shut off. Currents in the start-up circuit except for the one that flows through \( R_7 \) are shut down in normal mode operation.

6. Experimental results

The proposed circuit shown in Fig. 5 was fabricated using 0.35-μm CMOS technology. Figure 9 shows the chip microphotograph. The chip size is 2.5 x 2.5 mm². The voltage reference is formed as a part of the step-down DC-DC converter which needs 0.5 V of reference voltage and 13 μA of constant current source for achieving down to 0.7 V of DC-DC output voltage. There is no trimming for resistors because the reference voltage is completely determined by the resistor ratio as seen in equation (10). Only four chips were available to evaluate, and we observed ±9 mV of voltage deviation for the 500 mV of reference voltage. This is considered to be the resistor ratio variation. In order to obtain good matching property for diodes \( D_1 \) and \( D_2 \) in Figure 5,
dummy transistors are placed around them; however, the N value of this voltage reference is only 4, and the area for the diodes becomes relatively small compared with that for the power transistors and drivers, as can be seen in the photograph of Figure 9. By contrast, the resistors in $V_{REF}$ part occupy much more area, though there are resistors on the chip for other functions. This follows from choice of a resistor width of 20 µm as described above. The area for the resistors could be reduced to 1/16 of the present value if we could tolerate an increase in resistor ratio variation. Further study is required to discover how much we can reduce the total resistance value without increasing power consumption. Obviously, we cannot afford an N value greater than 60 such as in [6] and [7] as the diode area would become sixteen times larger.

6.1 Temperature and supply-voltage dependence of the reference voltage

Fig. 6 shows the temperature dependence of $V_{REF}$. The bold line shows the measurement data while the dotted line shows the circuit simulation data. The value of $V_{REF}$ was designed to be 0.5 V and with zero temperature coefficient at 25°C. The voltage change seen in Fig. 6 is approximately 3 mV over the temperature range from -55 to +75 degrees. As this 3 mV is 0.6% of the reference voltage of 500 mV, the temperature change is calculated as 46 ppm/°C. Simulation data also support the trend of this measurement. The peak voltage should appear at 25°C; however, it is shifted. We could compensate by adjusting $R_4$ in Figure 5. The curve resembles that of a bipolar bandgap voltage reference in shape, verifying equation (14) [5].

Fig. 7 shows the supply voltage dependence of $V_{REF}$. Again, the bold line is the measurement data while the dotted line is the simulation data. The supply voltage for the circuit in Figure 5 is the input voltage to the step-down DC-DC converter in this case, and it ranges from 2.4 V to 3.3 V. The design of this DC-DC converter has initially been done for supply voltage from 2.5 V to 5.5 V; however, it is limited to 3.3 V for the chip shown in Figure 9 due to the breakdown voltage constraint of the 0.35 µm CMOS process. From the measurement data, about 2 mV change of $V_{REF}$ was seen for a supply voltage change from 2.4 V to 3.3 V; that is 2.2mV/V, although it was much less in the simulation. The $V_{REF}$ change depending on the supply voltage largely depends on the voltage gain of the op-amp A1 in Figure 4. The result in Figure 7 indicates that the design was acceptable.

6.2 Temperature dependence of the constant current source

Figure 8 shows the temperature dependence of the constant current source that is needed in DC-DC converters to realize stable oscillation and control output voltage. The TC of the resistor is -2,600 ppm/°C. The current source value for Figure 8 is designed to be 13 µA. However, the peak point is shifted to the left, that is, to a lower temperature point; the current change is 6% in total for a 130 degree temperature change, which is larger than our expectation although it is within the specification of the DC-DC converter of 10%. The measurement data does not agree with the simulation data in the low-temperature region. Constant TCs are assumed for $V_{BED1}$, R5, and R6 for the calculation of TC cancelation to obtain the temperature dependent constant current source. This point will be improved in future work.
7. Conclusion

An IC voltage and current reference circuit with a reduced number of diodes used to generate multiples of $V_T$ and with low reference voltage of less-than-1 V has been proposed, designed, fabricated and evaluated using 0.35 µm CMOS devices. The aim was its eventual use in a low output voltage, and a low diode area for the step-down DC-DC converter IC. The evaluation results for both temperature and supply-voltage dependence for the 0.5 V voltage reference are acceptable while the temperature dependence for the 13 µA constant current source requires further improvement. We also need to optimise the chip area occupied by the resistors.

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References


Hiroki Sakurai received the B.E. and M.E. degrees in 2002 and 2004 from Chuo University, Tokyo, Japan. He is currently a Ph.D student at the Graduate School of Electrical, Electronic, and Communication Engineering of Chuo University. He is interested in design and new circuit development especially in mixed-signal LSIs such as high-speed and high-resolution D-to-A converters and low-voltage step-down DC-DC converters. Mr. Sakurai is a student member of the Institute of Electronics, Information and Communication Engineers of Japan.

Yasuhiro Sugimoto received the B.E. degree from Tokyo Institute of Technology, Tokyo, Japan, M.E. degree from University of Michigan, Ann Arbor, Michigan, and Doctor of Engineering degree from Tokyo Institute of Technology, Tokyo, Japan, in 1973, 1980, and 1991, respectively. He joined Toshiba Semiconductor Group in 1973, engaged in the development of analog VLSIs. Since 1992, he has been with the Faculty of Science and Engineering, Chuo University where he is now a professor in the Department of Electrical, Electronic, and Communication Engineering. His main interest is the design and development of new circuits in mixed-signal and RF LSIs. He is the recipient of the 1989 Best Papers Award of European Solid-State Circuits Conference and the 1998 IEICE Best Papers Award. He is the author of three books. Dr. Sugimoto is a senior member of the Institute of Electrical and Electronics Engineers, INC., a member of the Institute of Electronics, Information and Communication Engineers of Japan and the Japan Consulting Engineers Association.