7-6

A TV(UHF/VHF)/FM/AM Compatible Bi-CMOS 1GHz Single Chip PLL IC

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1. Introduction

Wide band single chip PLL IC is required for receiving the broadcasting signal from long wave to TV UHF on a radio cassette tape recorder and a car radio. Input signal ranges from 0.5MHz to I GHz in frequency. Existing bipolar PLL chips can satisfy this requirement easily although they always consume power (1),(2). On the other hand, NMOS approach has been taken to achieve low power and low cost characteristics. In its early stage, the input frequency could not reach to 1GHz (3), but finally it achieved the 1GHz operation with relatively low power (4). However, the use of submicron channel transistor and the supply voltage reduction from 5V to 3.3V are necessary in the case (4). We have achieved the single chip PLL that can handle the input signal from 0.5MHz to 1GHz with low power by using 2μm design rule Bi-CMOS technology. As the design rule can be greatly relaxed compared with the NMOS case, the Bi-CMOS chip can be easily introduced to the production lines nowadays and also exhibit the cost merit.

2. System Architecture

Fig. 1 shows the block diagram of the prescaler & PLL IC. There prepared 3 input terminals for voltage controlled oscillators. The UHF oscillator signal is first divided by 2 and is applied to the dual modulus prescaler. Although there exists 5 different input signals, the chip can handle them with the aid of internal switches. The pulse swallow method is used for the programmable counter and the dual modulus prescaler operates up to 500MHz. 2 phase detector outputs (DO1 and DO2) are prepared for TV and FM/AM voltage controlled oscillators. 4.5 MHz of the X-tal oscillation is divided by the 16-bit programmable counter and is applied to the phase detector as the reference signal. There exists 2 main busses on the chip. One is code bus and is used for the control of the operation mode. Another is data bus and is used for supplying data to various counters. Codes and data are usually applied via the serial-in terminal by a controller outside the chip. These codes and data can be monitored and be made use of at data output and serial-out terminals. 2 more signal input terminals and counters are prepared for the purpose of automatic tuning.

3. Bi-CMOS Circuit Design

It is usually preferable to use bipolar counters for the high frequency input because they show superior input sensitivity due to higher gain and less noise than MOS counterparts. This is the reason why bipolar elements for signal input amplifiers, the divide-by-2 counter, and the dual modulus prescaler have been used. This enables MOS parts operate in just around 5 MHz. The main drawback of bipolar circuits is that they consume power. This is solved by cutting off the current of the corresponding functional blocks when they are not active. The MOS analog switches are used to cut the lines between bias and bipolar circuits. Oscillator block is also composed of bipolar elements. This enables the oscillation level small and reduces undesired injection of noise. Inputs for automatic tuning are also bipolar to be able to handle the small input signals. Some of data outputs are again bipolar so that they can drive the external indicators directly. In this kind of system where bipolar and MOS functions are totally mixed, it is important to have effective level conversion between bipolar logic and MOS logic. Mixed Bi-CMOS circuits shown in Fig. 2 and Fig. 3 can well satisfy the requirement.

4. The Experimental Results

A wide band input Bi-CMOS PLL IC has been realized by using 2μm design rule Bi-CMOS circuit and process technology. The resultant chip performance is listed in Table 1. The chip can handle 7 input signals including tuning signals in the frequency range from 0.3MHz to 1 GHz. Supply current varies according as the operating mode selected so that unnecessary power dissipation can be avoided. Some of data output current reach to 6mA and help to drive external components.

Fig. 4 shows the minimum input sensitivity of the chip. Frequency range from 0.7MHz to 1 GHz is covered by switching among 5 modes. The degradation of the input sensitivity below 1MHz in AM Low mode is due to noise and is under improvement to ensure the 0.5MHz specification.

Fig. 5 shows the photomicrograph of the chip. Chip size comes to be 9 mm^2 including 600 bipolar and MOS elements plus 1,400 gates. It is installed in a shrink type DIP 30 pin package.

5. Acknowledgements

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6. References

1) R. Lawton, P. Gaussen, N. Cowley, "A 1GHz SINGLE CHIP PLL FOR TV", ICCE Digest of Technical Papers, pp. 122-123, June 1982.
2) Y. Oida, T. Ishioka, M. Nakai, K. Motoe, S. Shimizu, S. Sawa, T. Koyanagi and T. Tokumaru, "A Single Chip PLL IC with a 150 MHz Dual Modulus Prescaler", IEEE Trans. on Consumer Electronics, pp. 259-266, August 1983.
3) T. Yamada, Y. Tsuda, K. Itoh, "A 500 MHz PLL NMOS LSI", ISSCC Digest of Technical Papers,

pp.78-79, February 1983.
4) T. Yamada, S. Wada, S. Ito, Y. Suga, "A 1.2 GHz Single-Chip NMOS PLL", ISSCC Digest of Technical Papers, pp.24-25, February 1985.

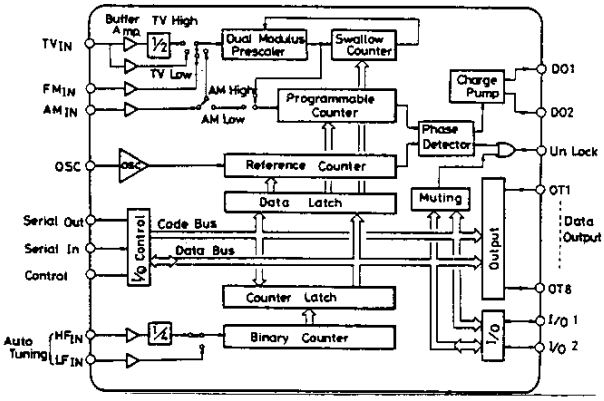

Fig. 1 Block Diagram of the Prescaler & PLL LSI

Item	Condition		Specification	Unit
Supply Voltage			+ 5.0 Single	V
Supply Current	TV High		60	mA
	TV Low		40	
	FM		35	
	AM High		30	
	AM Low		20	
Oscillator Frequency	—		1.0 ~ 15	MHz
Operating Frequency	V_{IN} = 150mVp-p	TV High	100 ~ 1000	MHz
		TV Low	50 ~ 500	
		FM	50 ~ 300	
		AM High	10 ~ 60	
		AM Low	0.5 ~ 20	
		Tuning High	5 ~ 60	
		Tuning Low	0.3 ~ 20	
Input Voltage Level	For All Modes		0.15 ~ 2.0	Vp-p
Data Output Current	OT1 ~ OT4		3	mA
	OT5 ~ OT8		6	
Phase Detector Output Current	High Level V_{OH} = 4V		- 2	mA
	Low Level V_{OL} = 1V		2	
DO Tristate Leak Current	—		± 0.1	μA
Chip Size	3.18 x 2.82			mm²
Elements Count	600 elements Plus 1,400 gates			—
Package	Shrink DIP 30 pin			—
Process	Single Metal 2 μm Bi-CMOS			—

Table 1 Chip Performance

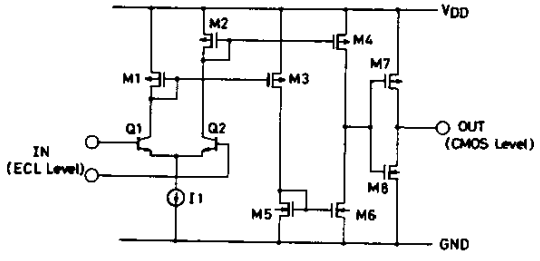

Fig. 2 ECL to CMOS Level Converter

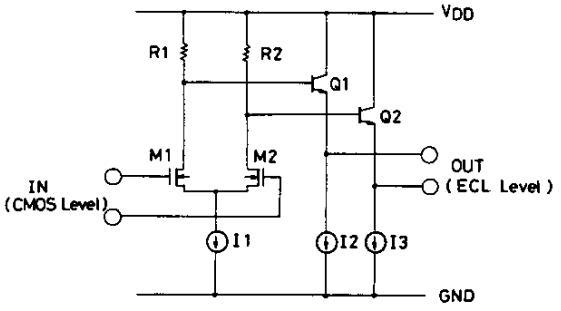

Fig. 3 CMOS to ECL Level Converter

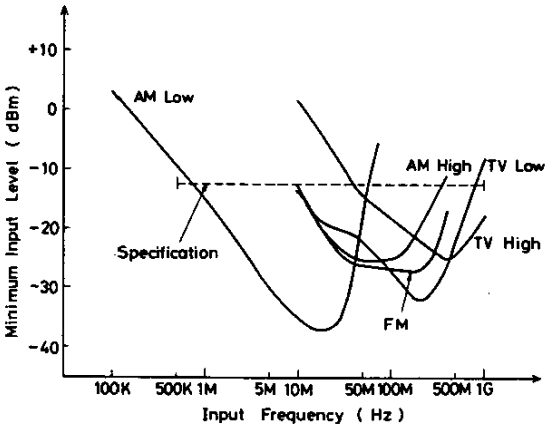

Fig. 4 Minimum Input Sensitivity

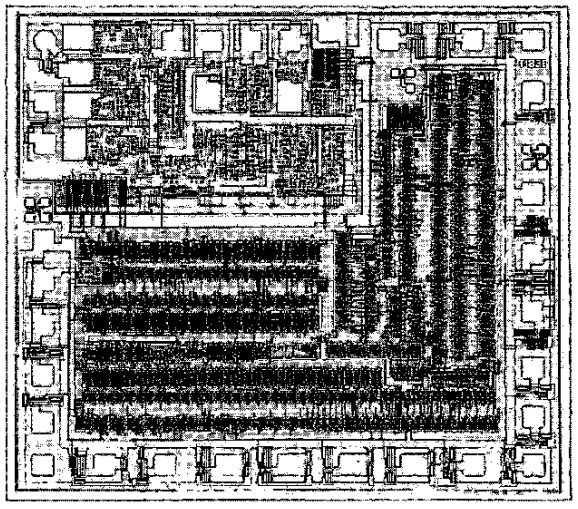

Fig. 5 Die Photograph