

# Special Correspondence

## An Experimental BiCMOS Video 10-Bit ADC

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**Abstract**—The possibility of realizing a high-quality, low-power, and low-cost video 10-bit ADC has been examined utilizing BiCMOS circuit and process technology. A single-power-supply, 10-bit, 10-MHz operation, 500-mW power dissipation, and a  $4.2 \times 6.2$ -mm chip size with 4200 elements are the results obtained.

### I. INTRODUCTION

Video-speed 10-bit ADC's have become more important than ever with the emergence of such a major application area as high-definition TV. There already exist flash-type video 10-bit ADC's realized by bipolar IC technology [1], [2]. However, they consume power and require a large chip area. Video speed 10-bit ADC's with subranging configuration have achieved lower power and less chip area [3], [4]. They need a high-speed precision sample-and-hold circuit [3], [4], an error amplifier, and a DAC [4]. If noise or droop exists at the sample-and-hold output, the subranging ADC without redundant correction bits in the fine ADC produces errors. The error amplifier also introduces errors to the fine ADC if the coarse ADC output is not correct. These require many redundant bits for the fine ADC [4]. The proposed subranging configuration in this paper eliminates the error amplifier and DAC and realizes less redundant bits for the fine ADC. Instead, error-free comparators and precise voltage transformation from coarse ladders to fine ones are required. A test chip adopting the new subranging configuration has been newly designed and fabricated. Bipolar comparators and MOS analog switches were used in an experimental video 10-bit ADC to fulfill the requirements. As a result of utilizing BiCMOS technology, single-power-supply operation, low power consumption, and small chip size have also been realized.

### II. LSI SYSTEM DESIGN AND NEW SUBRANGING ARCHITECTURE

The proposed system requires a sample-and-hold circuit in front of the ADC. A 10-bit linearity is required for the sample and hold. Fig. 1 shows a block diagram of an experimental BiCMOS video 10-bit ADC. The error amplifier and DAC, which appear in a conventional subranging ADC, have been eliminated by the use of MOS analog switches. A precise transformation of the reference voltage from coarse ladders to fine ladders is done by analog switches and buffer amplifiers.

Once one of the coarse comparators is activated, this forces the corresponding analog switches to be turned on. Then, the voltage range of 2 LSB's of the coarse ADC is transferred to the fine ladders. Next, the fine comparators are activated and perform comparison. Since there is a prepared redundancy in the fine comparators, code correction is performed in a later period if

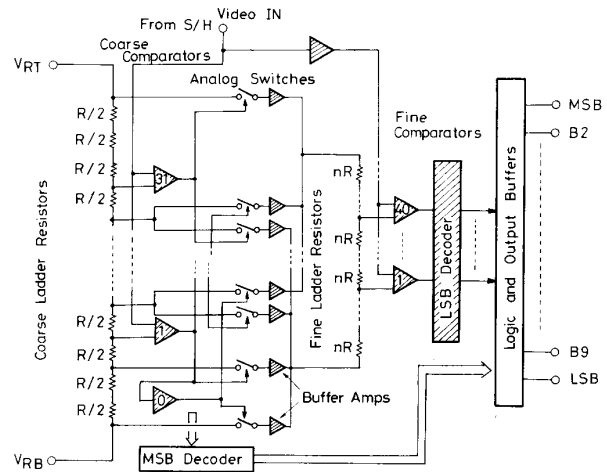


Fig. 1. Block diagram of BiCMOS video 10-bit ADC test chip.

necessary. A voltage transformation with a better than 1-mV precision is required because there is no amplification of the error voltage. The coarse-ladder resistors consist of  $80\text{-}\mu\text{m}$ -wide  $\text{MoSi}_2$  resistors in order to have less than 0.1-percent ratio. The analog switches and buffer amplifiers must not produce any voltage error. The buffer amplifier consists entirely of a bipolar emitter-follower circuit, and all the emitters are tied to each other to form a wired-OR circuit. The current flowing through this emitter follower is always kept constant and the variation in the voltage drop across it can be set to less than 0.5 mV. Although the base current of the bipolar emitter follower flows through the MOS analog switch, the voltage drop of each switch is small and constant in value because the emitter-follower current is constant. Inherently, there is no voltage drop across the switch, and the ADC can be designed to operate with a single power supply. Many redundant fine comparators are not necessary because precise voltage is transferred to the fine ladders.

Only eight redundant comparators were prepared. The necessity for preparing redundancy exists because there are 1) an offset between the buffered input signal and the transferred ladder voltage, and 2) clock harmonics and droop on the input of the ADC, which are generated periodically in synchronizing with the clock. Input voltage deviations within  $\pm 8$  mV can be corrected in this configuration. When the clock rate is increased, the transient in the fine-ladder settlement period begins to disturb the correct transformation of voltage. The redundancy can also help the situation. The coarse comparator also does not necessarily have a precise threshold because of this redundancy. The coarse ADC determines only the rough voltage range in which the input signal falls. Precise conversion is carried out when the fine comparators are activated. Therefore, a fine comparator must compare signals of less than 1.95-mV difference to perform a 10-bit conversion. High-speed capability is also required to operate in a high clock rate. The fine comparator consists entirely of bipolar devices to satisfy the requirements.

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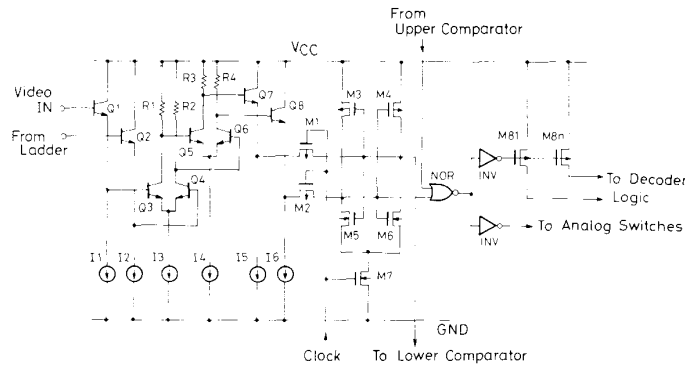


Fig. 2. Coarse comparator circuit.

### III. BiCMOS CIRCUIT DESIGN

The BiCMOS circuits were designed using the proposed sub-ranging configuration. Analog switches, logics, and output buffers were all CMOS, while the fine comparators, buffer amplifiers, and the bias circuit were all bipolar. Coarse comparators and level converters were mixed bipolar and CMOS.

The coarse comparator circuit is shown in Fig. 2. Although the coarse comparator did not need to have a precise threshold voltage, fast settling with a small input voltage in the sampling mode was necessary. The voltage applied to the CMOS latch must be large enough at the end of the sampling period. The amplifier part of the coarse comparator consisted of bipolar devices with a 36-dB gain, while the latch part consisted of CMOS devices to ensure rail-to-rail swing operation for controlling the analog switches. *M1* and *M2* in the figure are transfer gates and *M7* is a switch which cuts off the current of a latch during the sampling period of the comparator.

### IV. EXPERIMENTAL RESULTS

An experimental BiCMOS video 10-bit ADC was fabricated using a 3- $\mu\text{m}$  design rule BiCMOS process. The transit frequency  $f_T$  of the n-p-n transistor was 4 GHz. The transconductances of the NMOS and PMOS were 30 and 15  $\mu\text{S}/\mu\text{m}$ , respectively. The ladders consisted entirely of  $\text{MoSi}_2$  resistors with a sheet resistance of 5  $\Omega/\square$ . The evaluation of the ADC required an external sample and hold and a 10-bit video DAC. The ADC did not include the sample-and-hold function although it was necessary for this type of sub-ranging ADC. The external sample and hold used here had such features as 0.1-percent linearity, no droop, 0.5-percent differential gain, 0.5° differential phase, and 50-V/ $\mu\text{s}$  slew rate. Fig. 3(a) shows the linearity error which was measured by subtracting the reconstructed waveform from the input signal. The clock frequency was 7.5 MHz and vertical range for the error signal was 20 mV/div. The result shows that the error fell within 4 mV except in the overflow and underflow region. Overrange protection was not taken into account for this ADC chip, and therefore, the reconstructed waveform showed an abnormal figure in these regions. In the case of this sub-ranging ADC, the detection of overrange is necessary both in coarse and fine ADC's because code correction is adopted in the fine ADC. Another discontinuity has also been introduced near the right-hand side of the linear region. This is due to a mis-setup of the fine-ladder current around this region. When the input signal falls in between the 00000 and 00001 level of the coarse ADC, the coarse comparator and switch do not turn on. The system adds a

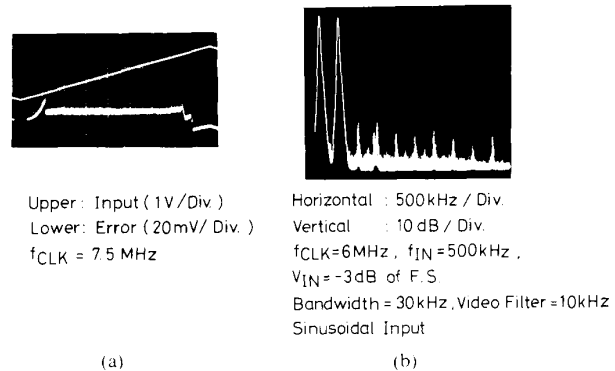


Fig. 3. Characteristics of reconstructed waveform: (a) linearity and (b) frequency spectrum.

TABLE I  
CHIP PERFORMANCE

Resolution	10 bits
Maximum Conversion Rate	10 MHz
Analog Input Range	3 to 5V
Power Dissipation	500 mW
Supply Voltage	+ 5V
Element Count	4,200
Chip Size	4.2 x 6.2 mm
Process	3 $\mu\text{m}$ Bi-CMOS Single Metal

logic and switches to treat this situation. The fine-ladder current in this region has been set to be different from that in other regions. Fig. 3(b) is a frequency spectrum of the reconstructed waveform when a 500-kHz input signal is applied. The noise level is observed to be about 75 dB below the input signal level with a 30-kHz bandwidth. This is equal to -60 dB of the noise level with a 30-MHz bandwidth. Although the level of the second and third harmonics can be observed as -57 dB below the input, this depends on the purity of the source signal generator and is not clear at this point. Table I summarizes the chip performance. A single-power-supply operation is realized. The maximum conversion rate was 10 MHz with a 500-mW power dissipation. The number of elements was only 4200 with a chip size of 4.2 x 6.2 mm. The fabrication process was 3- $\mu\text{m}$  BiCMOS with single metallization.

V. CONCLUSION

An experimental video 10-bit ADC has been designed and fabricated using BiCMOS circuit and process technology. The test chip does not include the sample-and-hold function. The new subranging configuration utilizing CMOS analog switches and bipolar high-speed high-accuracy comparators has been adopted. The results are a 10-bit 10-MHz operation, less than 4 mV of the linearity error, and -75 dB of the noise level with a 30-kHz bandwidth. The possibility of realizing a video 10-bit ADC has been confirmed. As the used design rule is only 3 μm, we can expect a higher frequency operation and a smaller chip size by using a further reduced version of the devices. Problems left for the future are to achieve 20-MHz operation, protection circuitry, and on-chip sample and hold.

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Using Active Components to Perform Voltage Division in Digital-to-Analog Conversion

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**Abstract**—A new design of a voltage-mode D/A converter using only fabrication steps required by the MOSFET's is described. The new D/A converter is implemented using a new basic-circuit-building block called the Three-Input AMPLifier (TIAMP) which can perform voltage addition and voltage division by two without using any passive component.

I. INTRODUCTION

General trends in the development of digital systems clearly predict the continuing emergence of highly complex, sophisticated, or "intelligent" chips. They will incorporate both complex digital assemblages and analog (sub) systems for interfacing and (possibly) special signal processing. Such on-chip analog (sub) systems certainly include A/D and D/A converters. But, since the digital system is likely to be complex and therefore to occupy most of the chip, any special fabrication steps required by the analog part will significantly impact the cost. Therefore, for such a hybrid chip, one needs analog techniques that do not use precise, well-matched, or highly linear passive components, nor employ corresponding processing steps unnecessary for digital circuits. This paper addresses the issue of such low-cost analog subsystems with emphasis on D/A conversion.

One important process of D/A conversion involves voltage division (by 2) and summation. Conventionally, voltage normally

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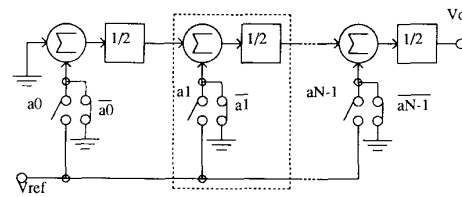


Fig. 1. D/A converter using voltage summers.

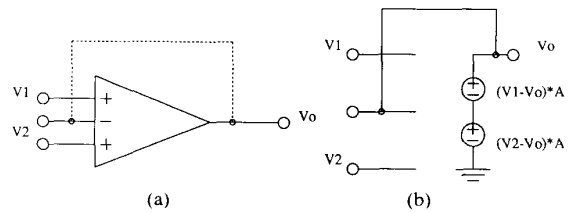


Fig. 2. (a) The TIAMP and (b) its equivalent circuit.

uses passive components. Consequently, at present, all voltage-mode D/A converters require linear well-matched components, resistors (nickel chrome), or capacitors (double polysilicon) whose processing cost is high.

In this paper, we describe a voltage-mode D/A conversion technique that eliminates the need for passive components in performing voltage division. Any fabrication process designed for digital circuits may be used to implement the proposed technique with accuracy appropriate for telecommunication applications.

II. A NEW D/A CONVERTER IMPLEMENTATION

Conceptually, the simplest and most straightforward form of D/A converter can be modeled as a cascade of voltage summers as shown in Fig. 1. Each summer sums the output of the preceding one with the ground potential or the reference voltage,<sup>1</sup> depending on the corresponding bit. Half the corresponding sum is provided as the output voltage of each stage. The output voltage of the entire D/A converter, which appears at the end of the amplifier cascade, may be written as

$$V_o = 1/2V_{ref} \{ a_{N-1} + a_{N-2}2^{-1} + \dots + a_12^{2-N} + a_02^{1-N} \}. \quad (1)$$

The long signal path traveled by the least-significant-bit (LSB) voltage requires the use of fast voltage summers to ensure a reasonable speed of operation. Nevertheless, for an accuracy better than 0.5 LSB, the LSB component of the output voltage of the D/A converter must settle only to 50 percent. Since all but the last of the voltage summers drive an internal node with very small parasitic capacitance, any reasonable amplifier with suitable compensation should allow operation at 100 kHz or above.

The only parameter that affects the (differential and integral) linearity of the D/A converter is the gain of the voltage summer. Modest accuracy requires the use of a voltage summer with reasonably well-controlled gain (for example, less than 0.2-percent gain error for an 8-bit accuracy).

It is obvious that the voltage summer may be implemented using operational amplifiers and a number of well-matched resis-

<sup>1</sup>In some cases, the ground potential may be varied to bias the voltage summer in a more linear region of operation.