BI-CMOS TRACKING SERVO LSI FOR 8 mm VCR

Satoshi Mizoguchi*, Yasuhiro Sugimoto*, Minoru Taguchi*,
Hiroshi Sadamatsu*, Tetsuo Hirota*,
Kiyoshi Nishitani**, Yoji Tanii**

*Semi conductor Division, Toshiba Corporation, Kawasaki, Japan
** Consumer Video Division, Sony Corporation, Tokyo, Japan

ABSTRACT

A tracking servo LSI for 8 mm VCR has been developed by utilizing 3 μm high-speed Bipolar CMOS technology. The chip contains analog functions such as a low noise amplifier, a gain control amplifier, balanced demodulators, rectifiers, a precision schmit amplifier and a subtracter, mixed analog-digital functions such as switched capacitor filters, sample & hold amplifiers and analog switches and digital functions such as an oscilator, a clock generator, counters and a externaly selectable 4 mode counter. Not only to realize mixed analog/digital functions easily but also high performance mixed analog/digital can be obtained when bipolar and CMOS devices are used in a circuit in a mixed manner. Integrating all necessary functions on one chip for a tracking servo system of 8 mm VCR, no adjustment and low power capability has been realized.

INTRODUTION

There exists several approaches to realize mixed analog/digital LSIs by using MOS technology, however, it is strictly difficult if precision analog functions such as low noise amplifiers and balanced demodulators are required. On the other hand, analog switches and switched capacitor filters are not suitable to realize when bipolar technology is used.

Especially in the tracking servo system of the 8 mm VCR, many mixed analog and digital functions are used. This means that the efficient mixture of high performance analog, digital and mixed analog/digital is required when the system is integrated on one chip. Only the bipolar-CMOS technology can correspond to the requirement because high performance bipolar and CMOS devices can be used in a mixed manner.

SYSTEM ARCHITECTURE

The block diagram of the newly developed tracking servo LSI for 8 mm VCR is shown in Fig. 1. The tracking information recorded on the tape is first applied to the low noise input amplifier. After passing through the gain control amplifier, the signal is applied to balanced demodulators in order to separate right and left side components in the tracking information. The switching frequency of balanced demodulators changes as the tape head moves to a different track. This switching signal is supplied by the externaly controlled programmable counter by dividing 5.9 MHz oscilator output from time to time. The demodulated right and left side tracking components are filtered out by 16.46 kHz and 46.2 kHz switched capacitor band-pass filter.

After amplifying, the signals are rectified and applied to the subtracter to produce the error signal. Switching of two components is necessary because 16.46 kHz and 46.2 kHz frequency components changes at every two tracks. The resulting error signal is then sampled and holded and put out to the motor driving part.

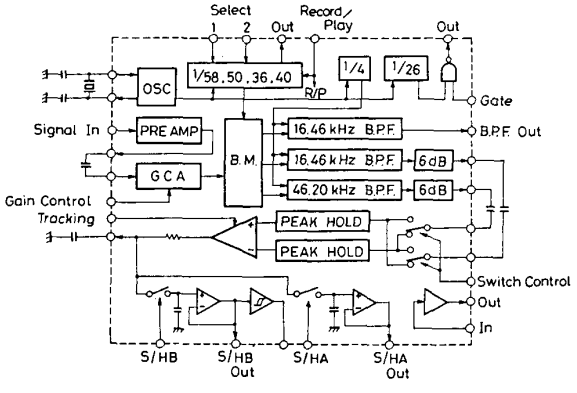

Fig. 1 Block diagram

IEEE 1988 CUSTOM INTEGRATED CIRCUITS CONFERENCE

CH2584-1/88/0000-0073 $1.00 © 1988 IEEE

Authorized licensed use limited to: Chuo University Library. Downloaded on January 27, 2010 at 04:39 from IEEE Xplore. Restrictions apply.

ANALOG PART

Analog part consits of a low noise amplifier, a gain control amplifier, balanced demodulators, analog switches, rectifiers, a subtracter and sample & hold amplifiers.

Care should be taken when the analog circuit is controlled by the digital signal. Fig. 2 shows the balanced demodulator circuit and its control scheme. As switching signal level applied to the demodulator imput should be small enough to ensure the proper operation, suppression of CMOS level swing is performed by first converting to BI-CMOS level and then to 1Vp-p swing divided by resistors.

Fig. 3 shows the circuit of the subtracter section. it consists of analog switches, rectifiers and a subtracter. A CMOS switch has excellent isolation characteristic and is very suitable to use for switching of analog signal. However, its equivalent on-resistance is not small that it is preferable to place in the base of a bipolar transistor. As the rectifier threshold level and its lineality and the production of the error signal are required to be precise, rectifiers and a subtracter consists totally of bipolar devices.

A low noise amplifier is of course consists of bipolar devices and its noise level is only -130 dBm at 100 kHZ.
1st Aluminum and poly-silicon layers are used for on chip capacitors. Sample & hold contains the 20 pF_2 on chip capacitor whose size is 40,000 μm^2. The operational amplifier used in the sample & hold is also mixed bipolar and CMOS type and has achieved high performance characteristics.

FILTER PART

The switched capacitor filter (S.C.F.) is the versatile filter because it can be installed on the chip easily by utilizing CMOS technology. But traditionally, the application has been limited to telephone

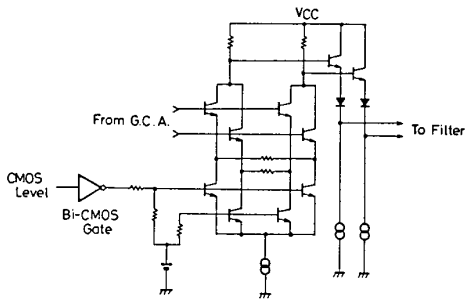

Fig. 2 Interface scheme between CMOS and analog in the balanced demodulator section

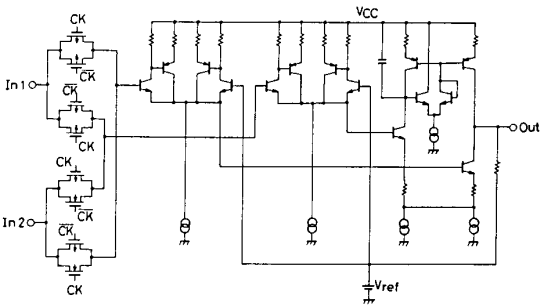

Fig. 3 Subtracter section

voice band signal processing owing to poor characteristics of CMOS operational amplifiers. By mixing bipolar and CMOS devices in the operational amplifier circuit, the high performance op-amp. can be obtained. As a result of this, the frequency range of the S.C.F. has extended to about 50 kHZ.

The chip contains three switched capacitor band-pass filters. Two of them have the center frequency of 16.46 kHZ and the other of 46.20 kHZ. These are positive second order type filters. Their clock frequency is 1.49 MHZ which is a one-fourth of the X'tal oscilator. Fig. 4

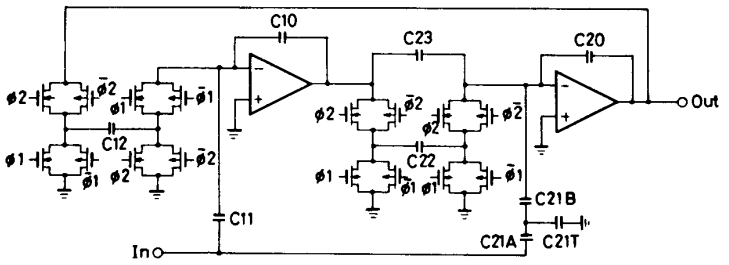

Fig. 4 Schematic of 46.20 kHz band-pass filter

Authorized licensed use limited to: Chuo University Library. Downloaded on January 27, 2010 at 04:39 from IEEE Xplore. Restrictions apply.

shows the circuit of the 46.20 kHZ band-pass filter. Each capacitor is the assembly of unit capacitors the size of which is 20 μm x 20 μm. To avoid the large capacitor ratio, T-type configuration has been adapted. Operational amplifiers used in S.C.F. must have low input current, high speed and low output impedance characteristics. The circuit is shown in Fig. 5. Bipolar devices are used both in input and output stages. From the noise point of view, it is preferable to use p-type MOS devices in the input. In order to ensure the P-MOS use and improve frequency characteristics, Q1 and Q2 are used in the input stage. Bipolar devices are also used in the output stage to lower the output impedance.

For the stable operation, compensation capacitors are also used as shown in the figure. Fig. 6 is the measured frequency characteristics. 80 dB of open loop gain and 6 MHZ of unity gain frequency has been obtained.

Fig. 7 and Fig. 8 are the results of 16.46 kHZ and 46.20 kHZ filter response respectively. Attenuation of 16.46 kHZ band-pass filter is more than 20 dB at 9 kHZ and 28 kHZ, and that of 46.20 kHZ filter is also more than 20 dB at 33 kHZ and 65 kHZ. The Qs of 16.46 kHZ and 46.20 kHZ band-pass filters are 12 and 30, respectively.
In each case, filter response is on the ideal curve and no degradation can be seen.

LOGIC PART

Logics on the chip are X'tal oscilator, a selectable 4 mode counter, 1/26 and 1/4 dividers.

BI-CMOS gates are used in the X'tal oscilator part to obtain the stable waveform at the frequency of 5.9 MHZ. Dividing ratio of the selectable 4 mode divider is either 58, 50, 36 or 40. This is controlled by the main servo LSI. 1/4 divider produces the clock frequency of the S.C.F.s. Non overlap clocks are produced in order to avoid degradation of the filter characteristic.

IC OUTLINE

Table-1 summarizes IC characteristics fablicated by 3 μm high speed BI-CMOS process. Power dissipation is 110 mW in play mode and 40 mW in record mode with 5V supply voltage. Elements count is 1400 and chip size is 3.28 x 3.28 mm^2. The chip is installed in 44 pin flat package. Die photograph is shown in Fig. 9.

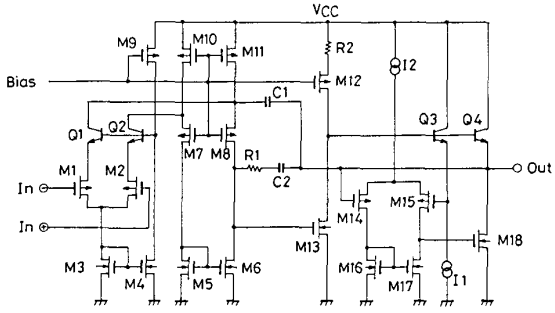

Fig. 5 Operational amplifier used in filter blocks

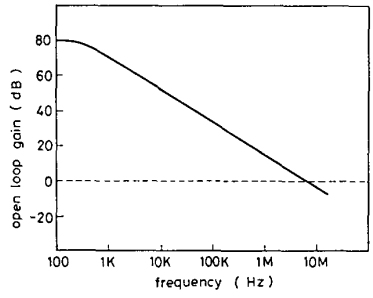

Fig. 6 Frequency characteristics of the operational amplifier in filter blocks

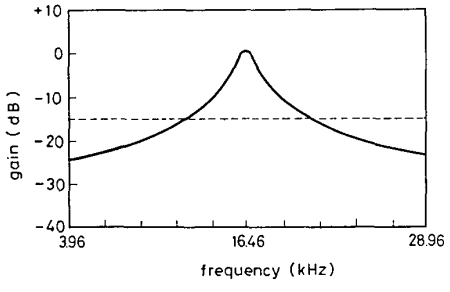

Fig. 7 Frequency response of the 16.4 kHz band-pass filter

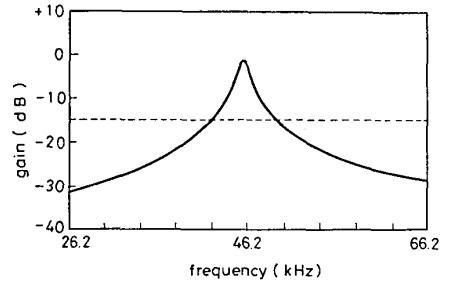

Fig. 8 Frequency response of the 46.20 kHz band-pass filter

Authorized licensed use limited to: Chuo University Library. Downloaded on January 27, 2010 at 04:39 from IEEE Xplore. Restrictions apply.

CONCLUSION

A tracking servo LSI for 8 mm VCR has been developed. The possibility of the co-existense of excellent analog function, mixed analog/digital function and logics has been verified by using BI-CMOS circuit and process technology. It has been turned out that BI-CMOS technology is very suitable for obtaining mixed analog and digital chips.

Reference

[1] R.W. Brodersen, P.R. Gray, and D.A. Hodges, "MOS switched capacitor filters," Proc. IEEE, Vol. 67, pp61 - 74, Jan. 1979.

[2] K. Martin, and A.S. Sedra, "Exact design of switched-capactitor bandpass filters using coupled-biquad structures," IEEE Trans. Circuit Syst. Vol. CAS-27, pp469 - 474, June 1980.

[3] T.C. Choi, R.T. Kaneshiro, R. Brodersen, P.R. Gray, W. Jett, and M. Wilcox, "High-frequency CMOS switched capacitor filter for communication applications," ISSCC Dig. Tech. Papers, pp246 - 247, Feb. 1983.

[4] T. Suzuku, H. Takatori, M. Ogawa, and N. Kunimi, "A CMOS switched-capacitor variable line equalizer," IECE Trans., Vol. J66-C, No. 12, pp951 - 958, Dec. 1983.

Table 1 Characteristics

Pre-amplifier Voltage gain Output noise level	 28dB -130dBm/Hz(at 100kHz)
Bandpass filter	
SCF switching clock frequency	1.49MHz
16.46kHz BPF Center frequency Q	 16.46kHz 12
46.20kHz BPF Center frequency Q	 46.20kHz 30
Supply voltage	5 V
Power dissipation Play mode Record mode	 110 mW 40 mW
Element counts	1400
Chip size	3.28mm×3.28mm
Fablication technology	Bipolar-CMOS
Package	Flat package 44pin

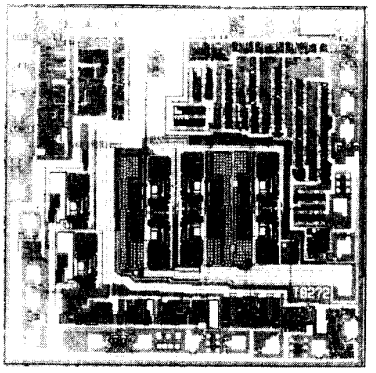

Fig. 9 Die photograph

Authorized licensed use limited to: Chuo University Library. Downloaded on January 27, 2010 at 04:39 from IEEE Xplore. Restrictions apply.