A Low-voltage and Stable Phase Compensation Technique to realize an 99 dB, 650 MHz and 1.8 V Three-stage Amplifier

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***Abstract*— A 1.8-V operational 3-stage Amplifier with a 99 dB of voltage gain, a 650 MHz of the unity-gain frequency bandwidth and 54 degrees of phase margin is realized. It has two pairs of a resistor and a capacitor in series as feedback elements and a feed-forward transconductance amplifier to perform threefold phase compensation. In order to apply this threefold phase compensation scheme to realize a high gain and high frequency 3-stage amplifier with enough phase margin, the small signal equivalent circuit model with stray capacitors at the output of each stage of amplifier is newly developed and the small signal transfer function including those stray capacitors are formulated. The transfer function is factorized into poles and zeros so that their relationship and influence on the frequency characteristics can be examined. The 3-stage amplifier is actually circuit designed by using 0.18μm CMOS devices. The calculated gain and phase frequency characteristics from our equivalent circuit model with stray capacitors have agreed very well with SPICE simulation results of the actual circuit especially at high frequencies above 1 GHz.**

I. Introduction

Our design target is a 3-stage amplifier which operates with a supply voltage of 1.8 V or less, has a high voltage gain of 96 dB or more and has a unity-gain frequency bandwidth of 622 MHz, so that the 3-stage amplifiers can be used as a sample-and-hold amplifier and an amplifier in the first bit-block of a high-resolution and high-speed pipelined ADC[1].

However, the output impedance of a reduced-size transistor becomes low due to the reduced gate length as LSI processes advance. The circuit technique such as a cascode or a buffered cascode configuration in order to enhance the output impedance and, therefore, to obtain high gain of the amplifier is no longer valid due to the constraint for the amplifier to operate in a 1.8 V or less of supply voltage. As the amplifier with only one stage no longer exhibits high voltage gain, 3 to 4 multiple stages of amplifiers are used to form the amplifier with more than a 96 dB of voltage gain[2].

The difficulty, however, does exist in the multi-stage amplifier due to the phase delay in a stage because it easily adds up to 180 degrees at a certain frequency when 3 or more amplifier stages are used. As the amplifier often operates with the 100 % negative feedback, the effective phase compensation method is really needed to stabilize the amplifier.

In this paper, we propose to use the phase compensation using two pairs of a resistor and a capacitor in series as feedback elements and a feed-forward transconductance amplifier in a 3-stage amplifier to realize low-voltage operation, high gain and high frequency characteristics with sufficient phase margin. Although the same phase compensation scheme appeared in reference 3, it was for an audio power amplifier which operated in a 5-V supply voltage and had only a 440 kHz of the frequency bandwidth using 0.35 μm CMOS devices. Moreover, there was no description for the voltage gain.

Therefore, it is not clear whether the proposed phase compensation scheme in reference 3 is really applicable to realize the high frequency amplifier with enough phase margins when stray capacitors at internal nodes should be taken into account. In this paper, we have tried to exploit the circuit design methodology for a high frequency amplifier using a 3-stage amplifier scheme. First, the small signal equivalent circuit of a 3-stage amplifier and its transfer function are constructed with stray capacitors at the output of each stage of an amplifier. The transfer function is factorized to poles and zeros so that their relationship and influence can be examined. As a result, it has turned out that two additional poles and one additional zero appear due to stray capacitors, and that they give strong influence on frequency characteristics at frequencies of a few times above the unity-gain frequency bandwidth. The 3-stage amplifier is actually circuit-designed and circuit-simulated by using 0.18 μm CMOS devices. The calculated values from our equivalent circuit model and SPICE simulation results of the designed circuit agreed very well in the gain and phase frequency characteristics especially at high frequencies above 1GHz. This means that our equivalent circuit model is effective in designing high frequency 3-stage amplifier with threefold phase compensation scheme.

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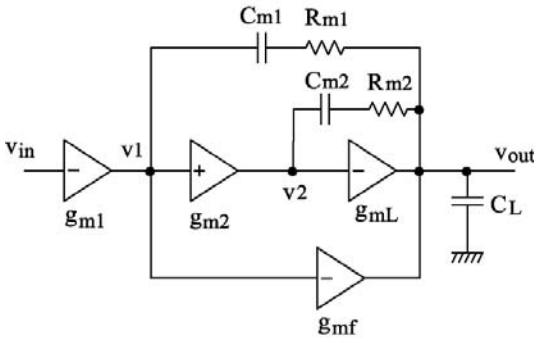

Fig. 1. Nested mirror compensation with feedforward gm stage and nulling resistors.

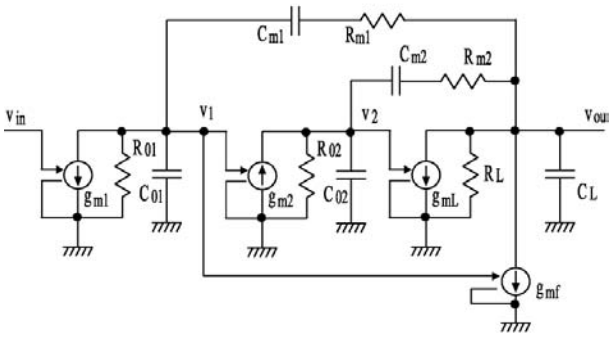

Fig. 2. The small-signal equivalent circuit of the circuit in Figure 1 with stray capacitors.

II. Phase compensation scheme in a 3-stage amplifier

The voltage gain of more than 96 dB can be obtained by cascading three of basic one-stage amplifiers. The 3-stage amplifier with the phase compensation using the 'Double nulling resistor compensation scheme' is shown in Figure 1. The amplifier by utilizing four or more stages of basic one-stage amplifier is seldom configured because the phase compensation becomes highly complex[4]. In Figure 1, g_{mf} stage, resistors R_{m1} and R_{m2} are prepared to produce zeros in the left half plane so that the 3-stage amplifier becomes stable. Therefore, the configuration shown in Figure 1 has the maximum phase margin compared with its counterparts[4].

The transfer function of the circuit shown in Figure 1 is derived from our newly established small signal equivalent circuit shown in Figure 2. In the previous work[3], the stray capacitor at the output of each g_m amplifier such as C_{01} or C_{02} is neglected assuming to be much less than the feedback capacitor such as C_{m1}, C_{m2} or C_L. However, in a high frequency amplifier, the value of C_{m1}, C_{m2} or C_L becomes small and, therefore, C_{01} or C_{02} can not be neglected. This is different from the discussion in the previous work. On the other hand, g_{m1}, g_{m2} and g_{mL} that are transconductances of amplifiers are much greater than the output conductance G_{01}, G_{02} and G_L. By applying the Kirchhoff's current law to independent nodes in Figure 2, the voltage transfer function $A_v(s) = v_{out}(s)/v_{in}(s)$ is calculated to become equation (1). Note that equation (1) has five poles and three zeros instead of three poles and two zeros in the previous work[3]. Two additional poles and one zero are produced by considering stray capacitors C_{01} and C_{02}.

Now, we would like to find each pole or zero location from equation (1) so that their relationship and influence can be examined. First, the pole locations were examined. At low signal frequencies, the Miller effect becomes dominant, and the dominant pole that associates with C_{m1} is introduced. As C_{o1} is outside the feedback loop as seen in Figure 2, its influence appears independently of other capacitors. At the v_1 terminal, the pole that associates with C_{o1} and resistors R_{o1} and R_{m1} in parallel is expected to produce a high-frequency pole, and this becomes the fifth pole in the denominator of equation (1).

The other three poles are from C_{m2}, C_{o2} and C_L. Their transfer functions are calculated by considering circuits with feedback loops, namely, those including the g_{m2}, g_{mL} and g_{mf} amplifiers shown in Figure 1. C_{m1} is shortened in this case. The influence of the Miller effect of C_{m2} with the inverting amplifier g_{mL} appears at middle frequencies, and the second pole is derived by considering C_{m2} only. At high frequencies, a small capacitor C_{o2} and a C_L which connects to a low impedance node such as the output of the g_{mL} amplifier, affect the frequency characteristics. The third and fourth poles are derived by considering C_{o2} and C_L. These poles are usually complex.

Next, zero positions are examined. Two pairs of a resistor and a capacitor in series as feedback elements shown in Figure 2 are highlighted as becoming two zeros in the middle signal-frequency range. We further found that the third zero appears due to the phase lag between v_1 and v_2 by the influence of C_{o2}. Feed-forward signals from v_1 through R_{m1}, from v_1 through g_{mf} amplifier and from the phase-shifted signal v_2 through R_{m2} will be combined at the output and becomes zero there.

Element values are chosen so that two poles except for the dominant pole in denominator and two zeros in the numerator in the transfer function cancel each other out. However, it is necessary to convert the complex third and the fourth poles in the denominator of equation (2) into real poles, at first. This is done by adjusting the R_{m2} value. Now, the second and third poles become real and form the second-order transfer function together. The coefficients of this second-order transfer function with those of the corresponding second-order transfer function of zeros in the numerator of equation (2) are compared and set equal to each other. As a result, the first and the second zeros and the second and the third poles in equation (2) are cancelled out. Again, this is done by adjusting R_{m1} and C_{m2}. The fourth pole is chosen so that it becomes more than two times the unity-gain frequency bandwidth in order to have a phase margin of more than 60 degrees. In this way, poles and zeros, and element values are decided.

$$A_v(s) = A_0 \frac{1 + s\left\{C_{m1}R_{m1} + C_{m2}\left(Rm2 + \frac{g_{mf}-g_{m2}}{g_{m2}g_{mL}}\right)\right\} + s^2 C_{m1}C_{m2}\left\{R_{m1}R_{m2} + \frac{R_{m1}\left(g_{mf}-g_{m2}\right)-1}{g_{m2}g_{mL}}\right\} + s^3 \frac{C_{m1}C_{m2}C_{o2}R_{m2}\left(g_{mf}R_{m1}-1\right)}{g_{m2}g_{mL}}}{1 + es + ds^2 + cs^3 + bs^4 + as^5}$$

$$a = C_{m1}C_{m2}C_L R_{o1}R_{o2}R_L R_{m1}R_{m2}C_{o2}C_{o2}, \qquad b = C_{m1}C_{m2}C_L R_{o1}R_{o2}R_L\left(C_{o1}R_{m1} + C_{o2}R_{m2}\right)$$
$$c = C_{m1}C_{m2}R_{o1}R_{o2}R_L\left\{C_L + C_{o1}g_{mL}R_{m1} + C_{o2}\left(1 + g_{mf}R_{m2}\right)\right\}$$
$$d = C_{m1}C_{m2}R_{o1}R_{o2}R_L\left(g_{m2}g_{mL}R_{m2} + g_{mL} + g_{mf} - g_{m2}\right), \qquad e = C_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L \tag{1}$$

$$A_v(s) \approx A_0 \frac{\left[1 + s\left\{C_{m1}R_{m1} + C_{m2}\left(Rm2 + \frac{g_{mf}-g_{m2}}{g_{m2}g_{mL}}\right)\right\} + s^2 C_{m1}C_{m2}\left\{R_{m1}R_{m2} + \frac{R_{m1}\left(g_{mf}-g_{m2}\right)-1}{g_{m2}g_{mL}}\right\}\right]\left\{1 + s\frac{C_{o2}R_{m2}\left(g_{mf}R_{m1}-1\right)}{R_{m1}\left(g_{mf}+g_{m2}g_{mL}R_{m2}\right)-1}\right\}}{\left(1 + sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L\right)\left\{1 + sC_{m2}\left(R_{m2} + \frac{g_{mL}+g_{mf}-g_{m2}}{g_{m2}g_{mL}}\right)\right\}\left(1 + s\frac{C_{o2}+C_L+C_{o2}g_{mf}R_{m2}}{g_{mf}+g_{mL}-g_{m2}+g_{m2}g_{mL}R_{m2}} + s^2\frac{C_L C_{o2}R_{m2}}{g_{mf}+g_{mL}-g_{m2}+g_{m2}g_{mL}R_{m2}}\right)(1 + sC_{o1}R_{m1})} \tag{2}$$

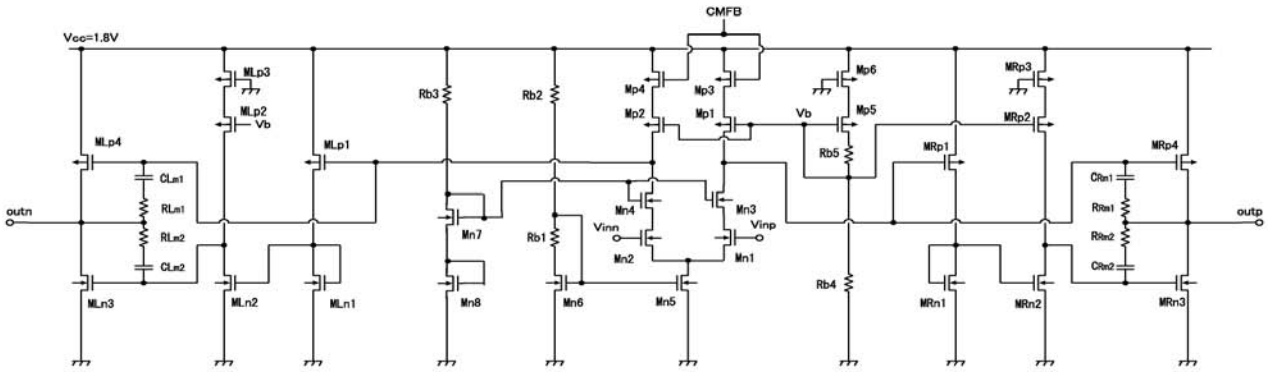

Fig. 3. The three-stage amplifier circuit.

III. The circuit of a differential three-stage amplifier

The fully differential configulation is necessary to use in our intended application such as an ADC. Figure 3 shows the circuit of the 3-stage amplifier which was designed using 0.18μm CMOS devices. The first-stage input amplifier, which corresponds to g_{m1} in Figure 2, consists of the cascode differential transistor pair of Mn1 to Mn4 with cascode current source transistors of Mp1 to Mp4 as loads. A common-mode feedback signal CMFB is applied to current source transistors Mp3 and Mp4. The input bias voltage is chosen to be 0.9 V from a 1.8 V power supply. The second-stage amplifier which corresponds to g_{m2} in Figure 2 consists of a PMOS transistor MXp1 (R for X means the right channel and L for X means the left channel) as an common-source amplifier and MXp2 as a load. MXp3 is a source degeneration resistor for MXp2, and MXn1 and MXn2 consists of a current mirror. This second amplifier stage has the positive gain. The third stage amplifier which corresponds to g_{mL} in Figure 2 consists of a transistor MXn3 and the feed-forward amplifier which corresponds to g_{mf} in Figure 2 consists of a PMOS transistor MXp4. The phase compensation circuit which consists of a series of C_{m1} and R_{m1} connects from the output of the third-stage amplifier to the output of the first-stage amplifier, while the other phase compensation circuit which consists of a series of C_{m2} and R_{m2} connects from the output of the third-stage amplifier to the output of the second-stage amplifier exactly in the same manner as shown in Figures 1 and 2.

IV. Simulation results and comparison

The proposed design methodology for a low-voltage operational, high gain and high frequency 3-stage amplifier with sufficient phase margin, which has taken high-frequency poles and zeros into consideration, has been examined by comparing the calculated frequency characteristics from the equivalent circuit model with SPICE simulation results of the designed transistor circuit.

The dotted line in Figure 4 shows the gain and phase frequency characteristics that are the calculation values based on the equivalent circuit model in reference 3, while the solid line shows the SPICE simulation results of the circuit shown in

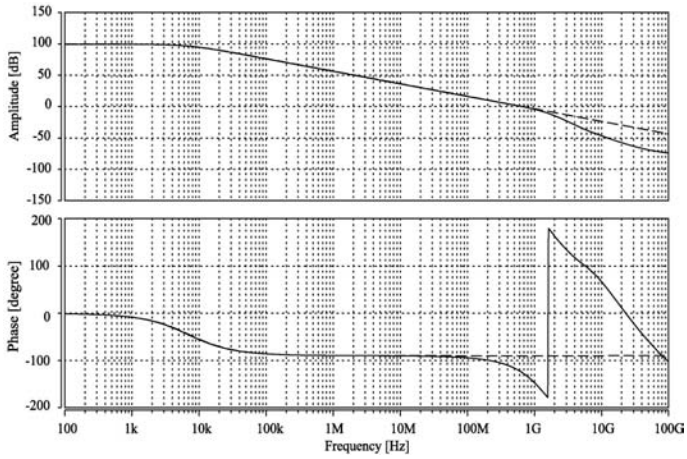

Fig. 4. The gain and phase frequency characteristics (dotted: equivalent circuit model from reference 3, solid: SPICE simulation result of the circuit in Figure 3).

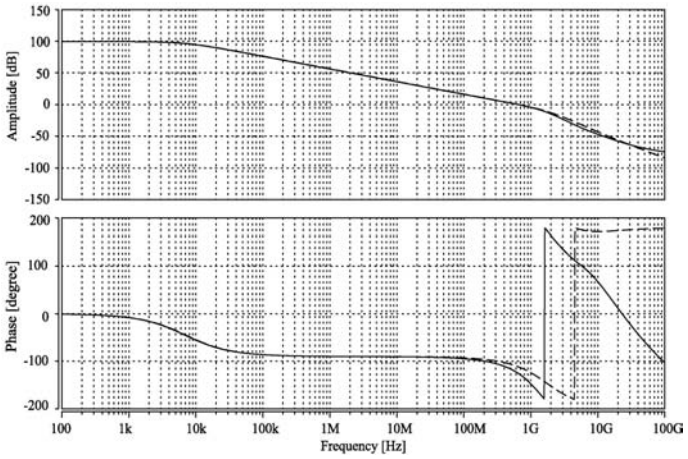

Fig. 5. The gain and phase frequency characteristics (dotted: equivalent circuit model in Figure 2, solid: SPICE simulation result of the circuit in Figure 3).

Figure 3. The equivalent circuit model in reference 3 does not have stray capacitors C_{01} and C_{02}. The small signal transfer function has three poles and two zeros, and one pole out of three poles is the dominant pole. Values of R_{m1}, R_{m2}, C_{m1} and C_{m2} have been decided so that the location of two poles and two zeros cancel with each other as described before. They are 120 Ω, 200 Ω, 1.9 pF and 0.5 pF, respectively. The rest of element values R_{01}, R_{02}, R_L, C_{01}, C_{02}, g_{m1}, g_{m2}, g_{mL} and g_{mf} are derived from SPICE simulation of the circuit shown in Figure 3 with maintaining the constraint of $g_{mf} > g_{m2}$. They are chosen to be 17.5 $k\Omega$, 27 $k\Omega$, 1 $k\Omega$, 0.5 pF, 0.1 pF, 8.1 mS, 2.4 mS, 10 mS and 14.9 mS, respectively. C_L is decided by the application and it is 4.3 pF which includes 0.3 pF of stray capacitance at the output terminal.

As a result, the first-order LPF characteristics with a low-frequency gain of 99 dB, a unity-gain frequency bandwidth of 660 MHz and a phase margin of 89 degree were obtained. However, as can be seen in solid line, the fall off of the gain and the additional phase lag are introduced to the actual circuit although the fall off can not be seen in the dotted line. In the case of the solid line, a low-frequency gain of 99 dB was obtained, however, a unity-gain frequency bandwidth and a phase margin degrade to 657 MHz and 54 degree, respectively. This means that we need to consider high frequency poles and zeros in actual circuit design.

We are proposing to take those high frequency poles and zeros into consideration in the equivalent circuit model so that the model can predict the unity-gain frequency bandwidth and the phase margin precicely to match with those of the actual circuit. Figure 5 compares the frequency characteristics between calculated values using the equivalent circuit model with stray capacitors shown in Figure 2 in dotted lines with the SPICE simulation result of the circuit shown in Figure 3 in solid lines. The curve from SPICE simulation result is the same one as the curve appeared in Figure 4. For the equivalent circuit model, a low-frequency gain of 99 dB, a unity-gain frequency bandwidth of 670 MHz and a phase margin of 67 degree were observed. Both curves in Figure 5 agreed very well up to frequencies above 1 GHz. It is clear that considering stray capacitors in our way is important. A phase shift at frequencies above 1 GHz in SPICE simulation result of the designed circuit is due to additional stray capacitors that are included in the actual circuit. We have not discussed about those additional stray capacitors in this paper, however, it is true that they degrades the phase margin about 10 degrees.

V. Conclusion

We have developed the design methodology of a 3-stage amplifier with two pairs of a capacitor and a resistor in series as feedback elements and with a feed forward transconductance amplifier to realize an amplifier with low-voltage, high-gain and high-frequency characteristics. We newly included stray capacitors at outputs of each stage amplifier in the equivalent circuit model of a 3-stage amplifier in the analysis of the transfer function, and found that the calculated frequency characteristics based on our approach is as precise as those from the actual circuit.

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