IEEE Asian Solid-State Circuits Conference
November 14-16, 2011 / Jeju, Korea

A MOS Current-Mode Boost DC-DC Converter with the Duty-Ratio-Independent Frequency Characteristics

Yuya Hirano
Graduate School of E.E. and C. Engineering
Chuo University
Tokyo, Japan
yhirano@sugi.elect.chuo-u.ac.jp

Yasuhiro Sugimoto
Department of E.E. and C. Engineering
Chuo University
Tokyo, Japan
sugimoto@sugi.elect.chuo-u.ac.jp

***Abstract*— In order to elevate an input voltage of less than 1-V to an output voltage of from several volts to 10-V while also realizing a large output-current capability, a wide feedback-loop frequency bandwidth under a high duty-ratio condition and a high power efficiency, we developed a MOS current-mode boost DC-DC converter which utilizes the quadratic compensation slope with the output voltage dependency and the variable gain amplifier in front of the error amplifier. The frequency characteristics of the total feedback loop were independent of the duty-ratio change. A test chip was fabricated by using a 0.18-um high-voltage CMOS process. The resulting 1 MHz operational MOS current-mode boost DC-DC converter converted input voltages of 0.4-V to 5.3-V to output voltages of 1-V to 6-V, realized 50 mA and 150 mA of output currents for input voltages of 1-V and 1.8-V, respectively, realized a feedback-loop frequency bandwidth of 70 kHz with a 1-V input and a duty-ratio of 81%, and realized 75% and 90% power efficiency for the 1-V and 2.5-V inputs, respectively, when the output voltage was 5.3 V.**

I. INTRODUCTION

Solar-cell panels consist of series or parallel connected unit-cells each made up of a p-n junction diode formed on a silicon wafer, and obtain an output voltage of 12 V or 24 V and a large output current capability. An individual unit-cell can only generate approximately 0.6 V output. The power efficiency degrades substantially when several unit-cells are connected in series because the power that can be taken out is limited by the unit-cell having the least power in the series. We propose a direct voltage transformation from the voltage of one or two unit-cells to the desired 12-V or 24-V. To accomplish this, it is necessary for the boost DC-DC converter to operate under a high duty-ratio such as 80% or 90%. A previous analysis has demonstrated that both the open-loop gain and frequency bandwidth in frequency characteristics of the feedback control loop in the current-mode boost DC-DC converter are reduced when the duty-ratio becomes high [1].

In order to eliminate the duty-ratio dependency on the frequency characteristics, we introduced the following quadratic compensation slope and the variable gain amplifier to the MOS current-mode boost DC-DC converter in blocks 2 and 3 as shown in Figure 1.

II. THE QUADRATIC COMPENSATION SLOPE

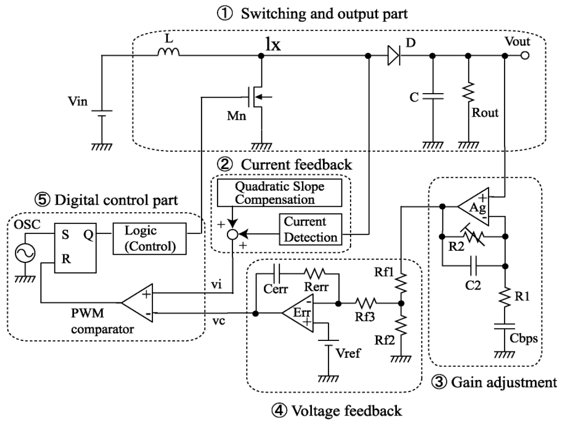


Figure 1. Block diagram of the designed MOS current-mode boost DC-DC converter.

A. The frequency characteristics of the standard DC-DC converter

The term standard indicates that it is the MOS current-mode boost DC-DC converter that uses the linear compensation slope. In this case, the duty-ratio dependency appears both in the current feedback loop and the output part. Figure 2 is a block representation of a MOS current-mode boost DC-DC converter using the small signal model. T_{cm} is the transfer function from the feedback voltage to the duty ratio, $T_{PS}G_{LCR}$ is the transfer function from the duty ratio to the inductor current, K_{cfb} is the current-to-voltage conversion gain from the inductor current I_L to the output voltage Vi of the current feedback part in Figure 1, $H_e(s)$ is the sampled-data transfer function, Z_{CR} is the transfer ratio from I_L to the output voltage Vout, β is the voltage-dividing ratio between resistors R_{f1} and R_{f2}, and $A_{err}(s)$ is the transfer function of the error amplifier. $T_{PS}G_{LCR}$ and Z_{CR} in the current feedback loop and in the output part, respectively,

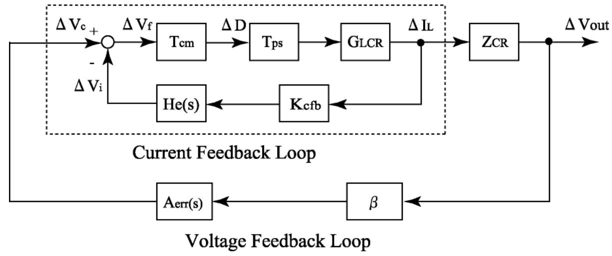


Figure 2. Small signal model of the current-mode boost DC-DC converter.

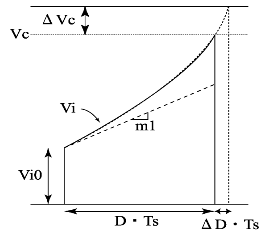


Figure 3. Waveform of Vi with a quadratic compensation slope.

are calculated using the state-space averaging method:

$$T_{ps}G_{LCR}=\frac{\Delta I_L}{\Delta D}=\frac{V_{out}}{(1-D)^2R_{out}}\times\frac{sCR_{out}+2}{s^2\dfrac{LC}{(1-D)^2}+s\dfrac{L}{(1-D)^2R_{out}}+1}$$

$$Z_{CR}=(1-D)R_{out}\times\frac{1-\dfrac{sL}{(1-D)^2R_{out}}}{sCR_{out}+2},\ H_e(s)\cong 1-\frac{s}{\omega_n Q_Z}+\frac{s^2}{\omega_n^{\,2}} \tag{1}$$

where D is the duty ratio that shows the time interval when the transistor Mn turns on, $\omega_n=\pi f_s$ and $Q_Z=-2/\pi$ [2].

From equation (1), it is found that both $T_{ps}G_{LCR}$ and Z_{CR} greatly suffer from the duty-ratio change.

B. Establishing the frequency characteristics of the current-feedback loop constant

We already know that the frequency characteristics of the current feedback loop including the $T_{ps}G_{LCR}$ function become constant if we use the quadratic compensation slope in the case of the buck DC-DC converter [3]. In this design, the same scheme is applied to form the boost DC-DC converter. We would like to examine whether this approach is effective. Now, the T_{cm} in Figure 2 should be in the form of the quadratic compensation slope. The waveform of Vi is shown in Figure 3. In a steady state, it becomes

$$V_i\big|_{t=DT_s}=V_c=m_1DT_s+m_c'(DT_s)^2+V_{i0} \tag{2}$$

where m1 is the coefficient of the converted voltage from the current that is proportional to the inductor current, mc' is the coefficient for the quadratic compensation slope, and Vi0 is the voltage of Vi at time zero. Ts is the period of the system clock. When Vc increases or Vi decreases by the amount ΔV_c as shown in Figure 3, we obtain

$$V_c+\Delta V_c=m_1(D+\Delta D)T_s+m_c'\{(D+\Delta D)T_s\}^2+V_{i0} \tag{3}$$

assuming that ΔD is sufficiently small compared with D. Tcm becomes

$$T_{cm}=\frac{\Delta D}{\Delta V_c}=\frac{f_s}{m+2m_c'DT_s},\ m_1=\frac{V_{in}K_{cfb}}{L} \tag{4}$$

Using the parameters in equations (1) and (4), the transfer function $T_{CFL}(s)$ of the current feedback loop, which is shown by the surrounding dotted lines in Figure 2, is calculated as

$$T_{CFL}(s)=\frac{\Delta I_L}{\Delta V_c}=\frac{T_{cm}T_{ps}G_{LCR}}{1+T_{cm}T_{ps}G_{LCR}H_e(s)K_{cfb}}$$

$$=\frac{1}{K_{cfb}}\times\frac{1}{1+\dfrac{2s}{\omega_n}\left\{\dfrac{L\left(m_1+2m_c'DT_s\right)\omega_n}{2V_{out}f_sK_{cfb}}-\dfrac{\pi}{4}\right\}+\dfrac{s^2}{\omega_n^{\,2}}} \tag{5}$$

$$=\frac{1}{K_{cfb}}\times\frac{1}{1+\dfrac{2s}{\omega_n}\varsigma+\dfrac{s^2}{\omega_n^{\,2}}}$$

Note that $T_{CFL}(s)$ is in the form of a 2nd-order low-pass filter. Moreover, only the damping factor ς becomes different from the case of the conventional linear slope [3]. We then obtain

$$\varsigma=\frac{\pi}{2}\left(\frac{V_{in}}{V_{out}}+\frac{2LDT_s}{V_{out}K_{cfb}}m_c'-\frac{1}{2}\right) \tag{6}$$

If we take the mc' value as

$$m_c'=\frac{V_{out}f_sK_{cfb}}{2L} \tag{7}$$

, then, the constant ς value of $\pi/4$ is obtained by substituting equation (7) into equation (6). This means that the frequency bandwidth of the current feedback loop does not change at any time. This is similar to the case of a current-mode buck DC-DC converter except that the Vout dependency of mc' takes the place of the Vin dependency.

Now, only Z_{CR} has the duty-ratio dependency. Calculating the loop transfer function $T_{out}(s)$ from ΔV_c to ΔV_{out} in Figure 2,

$$T_{out}(s)=\frac{\Delta V_{out}}{\Delta V_c}=T_{CFL}Z_{CR}=\frac{T_{cm}T_{ps}G_{LCR}}{1+T_{cm}T_{ps}G_{LCR}H_e(s)K_{cfb}}Z_{CR}$$

$$=\frac{(1-D)}{K_{cfb}}\times\frac{1}{\dfrac{(1-D)^2}{Lf_s}+\dfrac{2}{R_{out}}+sC}=\frac{(1-D)}{K_{cfb}}\times\frac{\dfrac{2Lf_s}{(1-D)^2}\,\|\,R_{out}}{2+sC\left\{\dfrac{2Lf_s}{(1-D)^2}\,\|\,R_{out}\right\}} \tag{8}$$

Here, the approximation

$$1>\frac{L}{(1-D)^2R_{out}}s,\ \frac{LC}{(1-D)^2}s^2,\ Z_{CR}\approx\frac{(1-D)R_{out}}{sCR_{out}+2} \tag{9}$$

was taken, because we are interested in the frequency range to a few hundred kHz when the clock frequency is 1 MHz..

Equation (8) shows that the loop gain from ΔV_c to ΔV_{out} changes depending on the duty ratio D, and it is the first order low-pass filter with the corner frequency that is decided by the parallel connection of the equivalent resistor $2Lf_s/(1-D)^2$ and the load resistor Rout. When Rout is large under a light loading condition, the corner frequency is largely dependent on the duty ratio.

However, we are stabilizing the frequency characteristics in the area when $2Lf_s/(1-D)^2$ is larger than Rout. In such an area, it is seen from equation (8) that $T_{out}(s)$ can be stabilized if (1-D) is inversely compensated. The corner frequency does not change much under a heavy loading condition because Rout is small. This is why the gain adjustment stage is newly added in advance of an error amplifier part as seen in Figure 1.

III. DESIGN OF THE QUADRATIC SLOPE GENERATION CIRCUIT

The circuits that are new to this MOS current-mode boost DC-DC converter compared with the previously developed MOS buck DC-DC converter are the quadratic slope generation circuit and the added gain adjustment circuit.

Figure 4 shows the circuit of the current feedback (CFB) part in Figure 1. The current that flows in M_n is equal to the inductor current when M_n turns on. When M_n turns on, the switch M_{sw1} is turned on and M_{sw2} is turned off, making voltages v_{cf1} and v_{cf2} of an operational amplifier A_2 equal to the drain-to-source voltage of M_n. As the gate voltage V_{clk} of transistor M_{nc} is set equal to the turn-on gate voltage of M_n, all the terminal voltages become equal for M_n and M_{nc}, and the current flowing in M_{nc} becomes proportional to the current flowing in M_n according to the size ratio of transistors. The current in M_{nc} is mirrored in the current I_{Lcpy} in M_2, and the control voltage that is proportional to the inductor current is obtained across R_{cfb}.

Transistors from M_{post1} to M_{post3}, SW_{sost} and a constant current source I_{ref2} together provide the offset current I_{ost} to R_{cfb} when SW_{sost} turns on in synchronization with M_n.

Transistors from M_{psl1} to M_{psl4}, M_{nslr}, capacitors C_{sl1} and C_{sl2}, a resistor R_{sl1}, operational amplifier A_1 and a constant current source I_{ref} make up the quadratic-compensation-slope generation circuit. When M_n turns on, SW_{sl1} and SW_{sl2} are turned off. I_{ref} is the constant current and is integrated twice by using capacitors C_{sl1} and C_{sl2}, producing a voltage proportional to t^2, where t is the time for integration. This voltage is applied to the drain of M_{nslr}. As M_{nslr} is driven in the linear operational region, its on-resistance becomes $1/\beta_{Mnslr}(V_{out}-V_{thMnslr})$. We obtain the quadratic slope I_{slope} as follows:

$$I_{slope}=\frac{I_{ref}\beta_{Mnslr}(V_{out}-V_{thMnslr})}{R_{sl1}C_{sl1}C_{sl2}}t^2 \tag{10}$$

Equation (10) indicates that the coefficient of I_{slope}, the coefficient mc' of the quadratic current, depends on the output voltage V_{out} provided that $V_{out}>V_{thMnslr}$. The combined current of I_{slope} and I_{Lcpy} which is proportional to I_L flows in R_{cfb} and produces the control voltage v_c.

The gain adjustment circuit is external in this design and is formed simply as shown in Figure 1 by using an operational amplifier A_g, a resistor R_1 and a variable resistor R_2, and one capacitor C_2. C_{bps} is just for by-pass. In reality, there appears one zero in the transfer function Z_{CR} as seen in equation (1) although we ignored this zero in equation (8) and (9). When the duty-ratio increases, this zero begins to appear in the frequency characteristics and we need to suppress it. The capacitor C_2 is used for this purpose. Depending on the duty-ratio that corresponds to the desired output, the gain of the gain adjustment circuit is set.

IV. EXPERIMENTAL RESULTS

The evaluation results of the test chip using 0.18-μm high-voltage CMOS process show the effectiveness of the proposed quadratic slope compensation and the gain adjustment schemes for a MOS boost DC-DC converter under high duty-ratio operation. The inductor L(10 μH), a capacitor C(10 μF), a load resistor R_{out}, the gain adjustment circuit A_g, R_1, R_2, C_2 and C_{bps}, feedback resistors R_{f1} and R_{f2}, and feedback elements of an error amplifier C_{err}(250 pF) and R_{err}(300 kΩ) in Figure 1 are all external components. The clock frequency is 1 MHz.

Figure 5 shows the frequency characteristics of the current feedback loop when V_{in} is fixed at 1.5 V and V_{out} changes from 3 V to 4 V to 5 V with a load current of 50 mA. Figure 5 indicates that the frequency characteristics of the current feedback loop do not change even when the duty-ratio changes; thus, the duty-ratio dependency is eliminated in the current feedback loop. In Figure 5, each curve was obtained by subtracting frequency characteristics of Z_{CR} from the measured frequency characteristics between output signals of the error amplifier (vc) and of the current-mode boost DC-DC converter (Vout) as shown in Figure 1. However, the duty-ratio dependency remains in the Z_{CR} part and is observed when the frequency characteristics of the total loop are displayed by changing the duty-ratios as shown in Figure 6. Here, the output current and voltage of the boost DC-DC converter are 40 mA and 5.3 V, respectively, and R_{out} is 120 Ω. The gain adjustment is not included. $2Lf_s/(1-D)^2$ is calculated as $20/(1-D)^2$ Ω. When the duty-ratio is increased, the gain decreases. However, the dominant pole does not seem to move, as indicated in equation (8), because $2Lf_s/(1-D)^2$ is larger than R_{out}. However, we observed a zero for the curve with the duty-ratio of 81% at a frequency of about 70 kHz.

Figure 7 shows the frequency characteristics of the total loop when the gain adjustment function is added to the circuit in Figure 6.

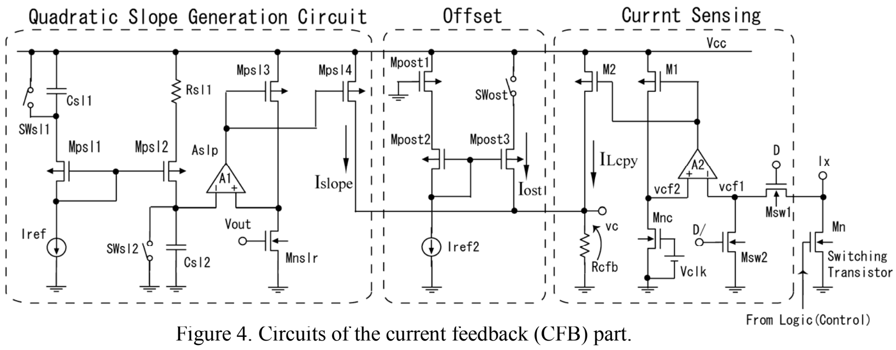


Figure 4. Circuits of the current feedback (CFB) part.

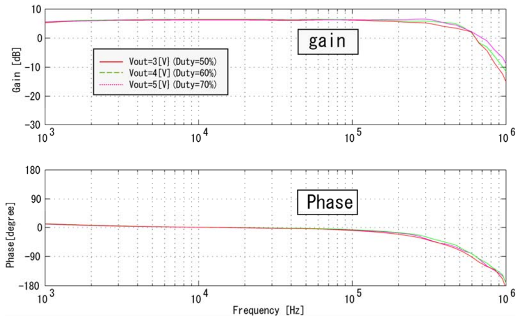


Figure 5. Gain and phase frequency characteristics of the current feedback loop with the fixed input and variable output voltages {Vin=1.5 V(fixed), Vout=3 V(D=0.5), 4 V(D=0.6) and 5 V(D=0.7)}.

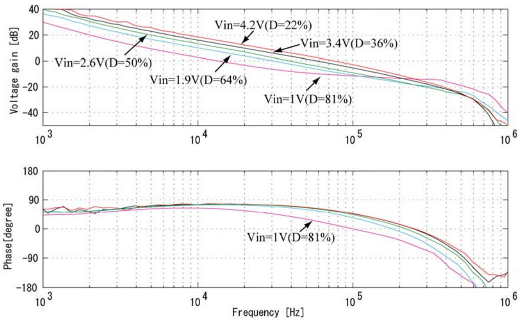


Figure 6. Frequency characteristics of the boost DC-DC converter without the gain adjustment function.

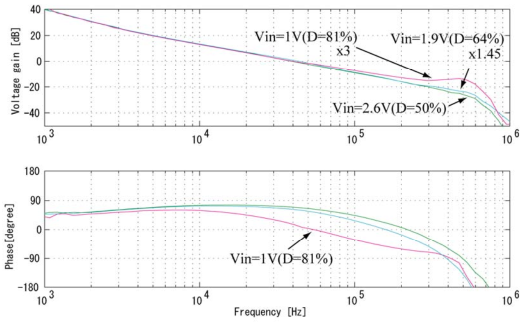
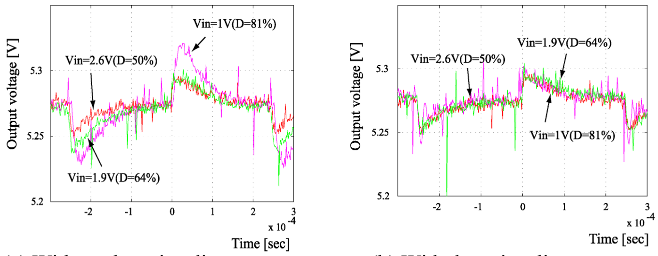


Figure 7. Frequency characteristics of the boost DC－DC converter with the gain adjustment function.

For the duty-ratios of 81% and 64%, the gain of 3 and 1.45 are chosen, respectively. As expected, the gain and phase become stable at frequencies below 70 kHz-that is, the frequency bandwidth. However, the effect of the zero as seen in Figure 6 seems to strongly affect the gain and phase frequency characteristics at frequencies above 70 kHz when the duty-ratio is 81%. Therefore, it turns out that we can not ignore the zero. This is a subject for future study.

Because the frequency characteristics and the frequency bandwidth become stable even when the duty-ratio changes, the transient response for the load current change must become stable. Figure 8 shows the transient response when the load current changes from 5 mA to 40 mA and vice versa. The output voltage is 5.3 V. Figure 8(a) is the case without the gain adjustment function when the duty-ratio changes from 51% to 64%, and then to 81%. An especially



(a) Without the gain adjustment (b) With the gain adjustment

Figure 8. The load current change from 5 mA to 40 mA and vice versa.

large output voltage-change is seen in the case with a duty-ratio of 81%. The voltage change and the time constant for the voltage decay increase when the duty-ratio increases. On the other hand, the output voltage change and the time constant in load current change become constant as seen in Figure 8(b), when the gain adjustment function is introduced. The effectiveness of the gain adjustment function is apparent. Finally, we summarize the chip performance in Table 1.

V. CONCLUSION

Constant frequency characteristics that do not depend on the duty-ratio change were achieved in a MOS current-mode boost DC-DC converter by applying the quadratic compensation slope in the current feedback loop and the gain adjustment function in the voltage feedback loop.

ACKNOWLEDGMENT

We thank VDEC (University of Tokyo) for the fabrication of this test chip.

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Table 1. Performance of a test chip

Input Voltage	0.4 V ~ 5.3 V
Output Voltage	1.0 V ~ 6.0 V
Max.Load Current	150 mA
Load Current Change	50 us (D: 50%~80%) less than 30 mV
Efficiency (In:2.5 V, Out:5 V)	90% (Iout=100 mA)
Process	0.18 um High-Voltage CMOS
Max.Voltage Tolerance	6 V