Linearity and Intrinsic Gain Enhancement Techniques using Positive Feedbacks to Realize a 1.2-V, 200-MHz, +10.3-dBm of IIP3 and 7th-order LPF in a 65-nm CMOS

Yasuhiro Sugimoto
Deptartment of Electrical, Electronic and Communication Engieering, Chuo University
1-13-27, Kasuga, Bunkyo-ku, Tokyo 112-8551, Japan
Tel: +81338171858, Fax: +81338171846, Email: sugimoto@sugi.elect.chuo-u.ac.jp

***Abstract*— Linearity and intrinsic gain enhancement techniques for realizing high-performance and low-voltage analog circuits in a deep-submicron CMOS are introduced. In place of a differential amplifier for the voltage-to-current (V/I) conversion at the input, a V/I conversion using a linear resistor and a positive feedback in a pseudo-differential configuration was adopted. The positive feedback concept was also applied to enhance the intrinsic gain of the deep-submicron MOS transistor which is used as a current source to realize high output impedance in amplifiers. In order to verify the effectiveness of the proposed techniques, a MOS 7th-order Gm-C linear phase low-pass-filter (LPF) was realized using a 65-nm CMOS process. Evaluation results showed that the -3 dB frequency bandwidth, group delay ripple, 3rd-order distortion and 3rd-order input intercept point (IIP3) were 200 MHz, 2.2%, less than -55 dB with a 100-MHz input and +10.3 dBm, respectively, all with a ±0.1 Vp-p signal input at each input terminal in pseudo differential configuration, while the LPF including an output buffer dissipated 60 mW from a 1.2-V supply.**

I. Introduction

The gate-leak problem and low supply-voltage operation are dominant obstacles for LSI circuits in deep-submicron CMOS processes [1]. However, the gate-leak problem can be avoided if the voltage applied to the transistor is suppressed as low as 1 V; this in turn introduces the low-voltage-operation issue. However, low-supply-voltage operation is hard for on-chip high-performance analog circuits because they suffer from extensive dynamic range reduction. Another serious problem in analog circuits is that the intrinsic gain (gm/gds), assuming the threshold voltage is kept constant, becomes very low in a deep-submicron transistor and the linearity degrades significantly in an amplifier.

To overcome these drawbacks, we propose the use of a linear resistor with applied positive feedback to convert the input signal voltage into current at the amplifier's input, instead of using a conventional differential circuit. The configuration in pseudo-differential form provides good linearity of the converted differential signal current under low-supply-voltage conditions. We further propose the use of positive feedback to increase the output impedance of a cascode current source at the output part of an amplifier. The high output impedance of the current source leads to high voltage gain and high linearity in a low-voltage amplifier. As a result, a low-voltage and high-performance transconductance amplifier could be realized. In order to verify the effectiveness of our proposal, a 7th-order Gm-C linear phase filter in a 65-nm CMOS process was fabricated. A new filter block configuration for a differential second-order LPF was developed and adopted. To compensate for the process, voltage and temperature (PVT) variation of transistors, capacitors and resistors, the programmability of the capacitors and resistors by the external control signal was ensured.

II. Transconductance amplifier design

In our filter, two transconductance amplifiers were used to form a second-order LPF. We designed the input part of the transconductance amplifier to realize 1.2-V operation, a -3 dB frequency bandwidth of 12 GHz and a THD of -68 dB with a ±0.1 Vp-p input at 100 MHz at each input terminal in pseudo differential configuration by simply carrying out the input V/I conversion using a linear resistor, positive feedback and a common gate transistor, as shown in Figure 1(a). We have already proposed the same type of linearity enhancement

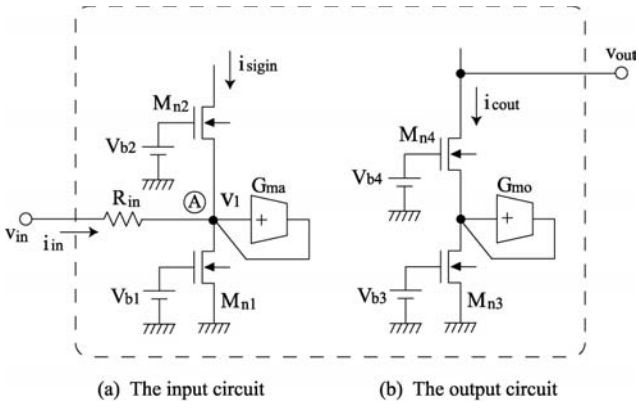

Fig. 1. Transconductance amplifier circuit. (a) Transconductance is linearized at the input. (b) Impedance is increased at the output.

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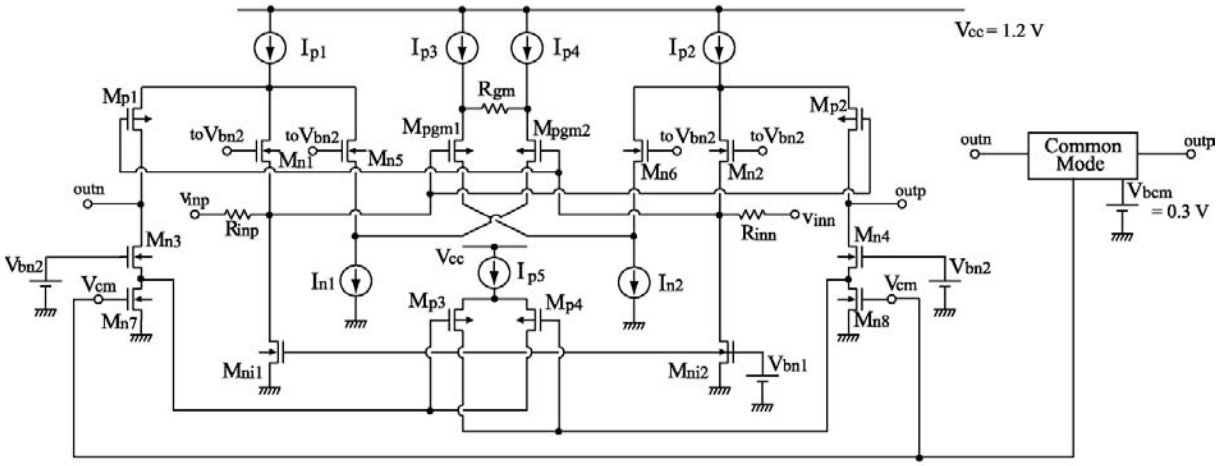

Fig. 2. The circuit of a transconductance amplifier.

technique [2], but an internal amplifier A1 as shown in Figure 1 of reference 2 was not used in the design described in this paper; and this modification avoids the generation of the peaking in frequency characteristics. In addition to this, a part of G_{ma} consists of a linear resistor to obtain matching partially to R_{in}. The following formula holds in Figure 1(a):

$$i_{sigin} = -G_{in}v_{in} + (G_{in} + g_{ds1} - G_{ma})\, v_1 \qquad (1)$$

where transistors M_{n1} and M_{n2} form a cascode current source and the signal is applied to the source terminal of M_{n2}. The i_{sigin} is the signal current that flows into M_{n2} and is output to the next stage of circuits, v_1 is the signal-dependent nonlinear voltage deviation generated at terminal A , g_{ds1} is the output conductance of M_{n1}, $G_{in} = 1/R_{in}$, and G_{ma} is the transconductance of a positive feedback circuit. If G_{ma} is set equal to $(G_{in} + g_{ds1})$, i_{sigin} becomes perfectly proportional to G_{in}.

In addition to the linearity issue in the V/I conversion at the input, there is a problem for the low-voltage transconductance amplifier such that the output impedance becomes very low. This is because the output impedance of the deep-submicron transistor in the current source is very low, and its drain-to-source voltage becomes low under the low-voltage operating condition. A cascode current source configuration is not sufficient to solve this problem. Mobarak et al. tested the use of negative resistance to increase the output impedance of the current source [3], but the linearity was degraded in that case. We used an appropriate positive feedback instead, as shown in Figure 1(b). The operation is formulated as

$$\begin{aligned} z_{out} &= \frac{v_{out}}{i_{cout}} = \frac{1}{g_{ds4}} \left\{ 1 + \frac{g_{m4} + g_{mbs4} + g_{ds4}}{g_{ds3} - G_{mo}} \right\} \\ &\approx \frac{1}{g_{ds4}} \left(1 + \frac{g_{m4}}{g_{ds3} - G_{mo}} \right) \end{aligned} \qquad (2)$$

Here, z_{out} is the output impedance seen from the v_{out} terminal into the current source, g_{ds3} and g_{ds4} are the output conductances of M_{n3} and M_{n4}, respectively, g_{m4} and g_{mbs4} are the gate and bulk transconductances of M_{n4}, respectively, and G_{mo} is the transconductance of the positive feedback circuit. If G_{mo} is set equal to g_{ds3}, then z_{out} becomes infinite. However, we need to be careful that G_{mo} does not exceed g_{ds3}. This condition may occur with PVT variation. To avoid this, the current source in G_{mo} is set to be manually tunable at present.

Using positive feedback, we designed a transconductance amplifier, as shown in Figure 2. The input positive-feedback circuit consisted of M_{pgm1}, M_{pgm2}, I_{p3}, I_{p4} and R_{gm}. The impedance of current sources M_{n7} and M_{n8} was increased by the positive-feedback circuit consisting of M_{p3}, M_{p4} and I_{p5}. As positive-feedback circuits at both the input and output are differential, they do not have the ability to improve even-order harmonics, while odd-order harmonics are suppressed. The whole circuit was configured as a pseudo-differential circuit, and thus the even harmonics were suppressed. Differential input voltage signals were applied to resistors R_{inp} and R_{inn}. The dc voltage of the output terminals $outp$ and $outn$ were chosen to be 0.3 V, and the common mode feedback circuit was prepared to regulate the common mode voltage at $outp$ and $outn$ by adjusting the current in M_{n7} and M_{n8}.

III. The filter design

A high-frequency and low-voltage 7th-order linear phase LPF was designed using the transconductors described in section II. Figure 3 shows a block diagram and the target IC specification. The filter has three Biquad (2nd-order) LPFs and one 1st-order LPF. The first Biquad LPF has a quality factor (Q) of 2.02 and a natural frequency of 463 MHz. It has a 6-dB peak at 463 MHz. The block structure in Figure 3 is the same as that described by Martinez et al [4]. However, we expected innovative characteristics such as an operation voltage of 1.2 V, a group delay ripple of less than 5% and a distortion level of -50 dB or less for a 50-MHz input when a 200-mV peak-to-peak amplitude at each input terminal in pseudo differential configuration is applied. Moreover, in reference 4, four transconductance amplifiers and four capacitors are used

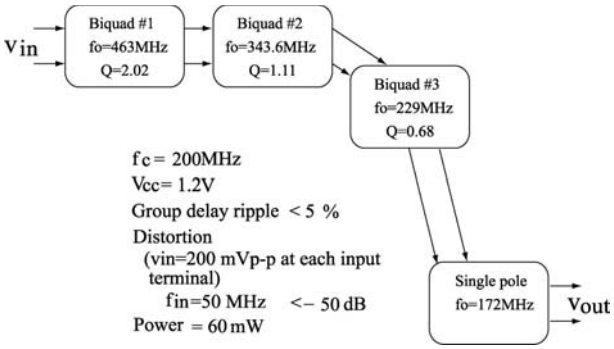

Fig. 3. Block diagram of the targeted 7th-order linear phase LPF.

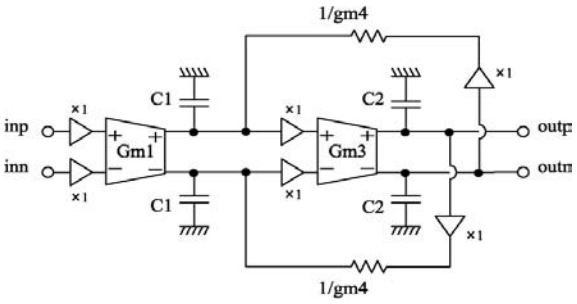

Fig. 4. The developed configuration of the 2nd-order LPF.

to form a Biquad LPF. In contrast to this previous design, we introduced a simplified Biquad LPF by replacing the transconductors with resistors, as shown in Figure 4. Note that we needed to put triangular-shaped buffers to drive and supply enough current to the resistor. However, we still obtained a small element count and a larger phase margin than in the previous design by eliminating complex transconductor amplifiers. Providing that the gain of the triangular-shaped buffer is unity, then the transfer function $H(s)$, the dc voltage gain A_0, natural frequency ω_0, and Q factor in this new configuration becomes

$$H(s) = \frac{G_{m1}}{g_{m4}} \cdot \frac{\frac{G_{m3}g_{m4}}{C_2C_1}}{s^2 + \frac{g_{m4}}{C_1}s + \frac{G_{m3}g_{m4}}{C_2C_1}}$$

$$A_0 = \frac{G_{m1}}{g_{m4}}, \quad \omega_0 = \sqrt{\frac{G_{m3}g_{m4}}{C_1C_2}}, \quad Q = \sqrt{\frac{G_{m3}C_1}{g_{m4}C_2}} \qquad (3)$$

Equation (3) indicates that A_0 and Q do not change even when the values of g_{m4}, G_{m1} and G_{m3} change due to the PVT variation because all of their values are decided by resistors that have the same variation characteristic, while ω_0 does change due to the lack of the tracking capability between a transconductance and a capacitor. The adjustment capability of capacitors C_1 and C_2 and a resistor $1/g_{m4}$ is provided by selecting one resistor out of several feedback resistors in parallel and connecting small capacitors in parallel using MOS switches controlled by an external signal.

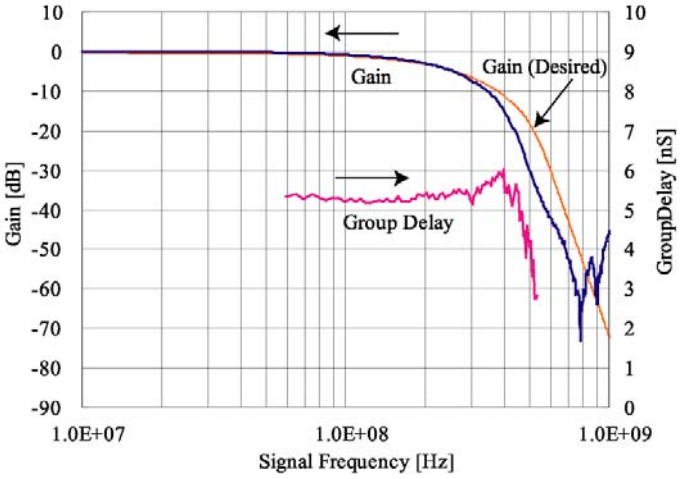

Fig. 5. Frequency characteristics and the group delay of the 7th-order LPF.

IV. Experimental Results

The 7th-order LPF shown in Figure 3 was designed, fabricated and evaluated using 65-nm CMOS devices. The drain-to-source resistance of a transistor with the gate length and gate width of 65 nm and 19.5 μm, respectively, was simulated to be 1.5 kΩ when the drain-to-source voltage was 0.25 V in the saturation region. The power dissipation of this 7th-order LPF was 60 mW, which includes output buffers from a 1.2-V supply. The core chip size was 0.5 mm$\times$0.7 mm.

Figure 5 shows the measured frequency characteristics of the voltage gain and group delay of the 7th-order linear phase LPF. The corner frequency, fc, was 200 MHz and the gain characteristics agreed well with the theoretical value up to 300 MHz. The group delay ripple was calculated to be 2.2% by using the formula

$$Group\ Delay\ Ripple = \frac{Max\left[\tau\left(f\right)\right] - Min\left[\tau\left(f\right)\right]}{Max\left[\tau\left(f\right)\right] + Min\left[\tau\left(f\right)\right]} \qquad (4)$$

where Max and Min are the maximum and minimum values of the group delay $\tau\left(f\right)$ in the frequency range from $0.3f_c$ to f_c [7].

Figure 6 displays the frequency spectrum up to 500 MHz when a $\pm$100 mVp-p and a 100-MHz input signal was applied at each input terminal of the 7th-order linear phase LPF. As the filter is configured in pseudo differential form, the input signal level is considered equivalent to be $\pm$200 mVp-p. As described in section II, the even-order harmonics were suppressed not in the transconductance amplifier but in the pseudo-differential configuration. The second harmonic can not be fully attenuated only by the pseudo-differential configuration. It was observed to be -51.88 dB relative to the output signal and was the largest in harmonics. The incompleteness of the common-mode feedback in a transconductor amplifier may produce even-order harmonics. In contrast, a very low third harmonic below -55 dB was obtained.

Figure 7 shows the result of the two-tone inter-modulation test using 99-MHz and 101-MHz input signals. The input

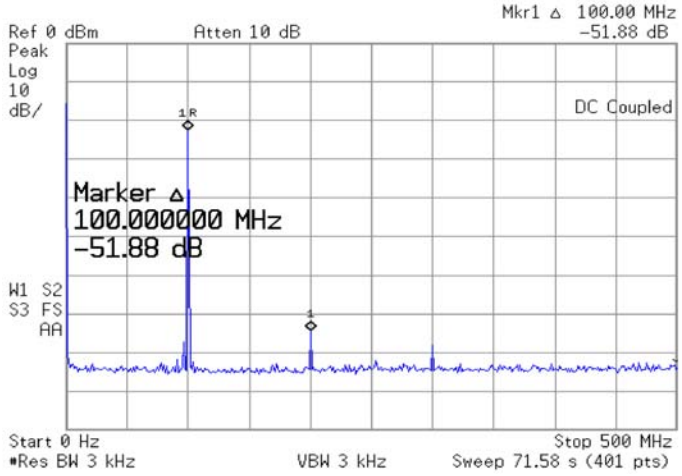

Fig. 6. The frequency spectrum up to 500 MHz with a full-scale 100-MHz signal input.

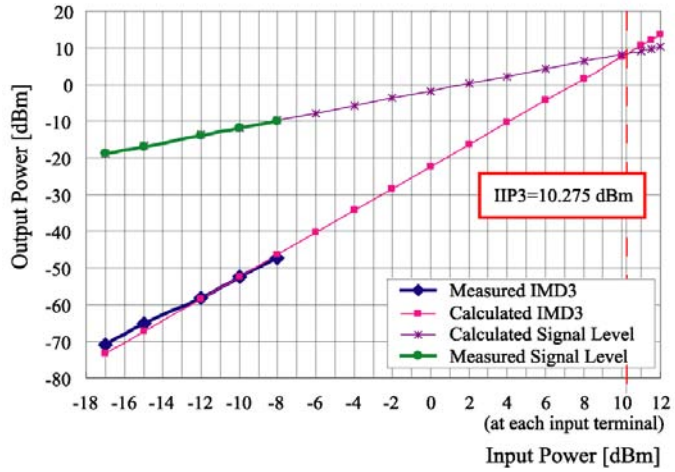

Fig. 7. The 3rd-order input intercept point (f_{in1}=99 MHz, f_{in2}=101 MHz).

power is the sum of the power of two signals. When the sum of two signal powers was set to -10 dBm at each input terminal in pseudo differential configuration, which is the full-scale input signal power at each input terminal, the measured 3rd-order distortion was -40.17 dB. The calculated IIP3 value became +10.3 dBm. If we take differential signals into account, it becomes equivalent to be +16.3 dBm. This large IIP3 value also meant that a highly linear operation was achieved under the condition of being forced to tolerate very low output resistance of a transistor and a low supply voltage of 1.2 V or less.

Finally, Table 1 compares the performance of this work with those of various prior low-pass-filters. As there is a lot of figure-of-merit (FoM) definitions, the FoM term is not included in the table. The group delay ripple is the least. The 3rd-order distortions (HD3) seen in Figure 6 and IIP3 are superior to those of other designs, considering that the filter order is as large as 7 and the supply voltage is as low as 1.2 V. The dynamic range is in the same level as those of other designs except for that of reference 3 with the supply voltage of less than 1.5 V. The noise level is almost the same as that of reference 4, while the supply voltage is almost one-third in our design. Although many resistors are used, the noise level is not large, however, it may become difficult to reduce the noise more. This should be the matter for future study.

Table 1. Performance comparison of a test chip

Reference	[4]	[5]	[6]	[3]	This Work
CMOS Technology	0.35um	65nm	0.18um	0.13um	65nm
Filter Order	7	5	4	2	7
-3dB Frequency	200MHz	275MHz	1GHz	200MHz	200MHz
Group Delay Ripple	<4% @fc	–	<4% @1.5fc	–	<2.2% @fc
HD3	<-44dB @500mVp-p fin=30MHz	–	IM3 <-43dB @350mVp-p fin=1GHz	IM3 <-31dB @750mVp-p fin=150MHz	<-55dB @400mVp-p differential fin=100MHz
IIP3	–	-12.5dBV (+0.5dBm)	–	+14dBm	+10.3dBm
DR	50 dB	44 dB	39 dB	54.5 dB	45 dB
Input Refered Noise	89 nV/$\sqrt{\text{Hz}}$	7.8 nV/$\sqrt{\text{Hz}}$	–	35.4 nV/$\sqrt{\text{Hz}}$	70 nV/$\sqrt{\text{Hz}}$
Supply Voltage	±1.5V	1.2V	1.5V	1.2V	1.2V
Power Consumption	60mW	36mW	175mW	20.8mW	60mW

V. Conclusion

A high-speed and high-performance analog circuit was realized by applying positive feedbacks and using a 65-nm CMOS with the characteristic of very low output-resistance in a deep-submicron transistor under a low-supply-voltage condition such as 1.2 V.

Acknowledgment

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