A Highly Efficient Transient and Frequency-Response Simulation Method for Switching Converters without Using a SPICE-like Analog Simulator

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Abstract— **This paper introduces and proposes a transient and frequency-response simulation method for switching converters that is both fast and precise; this method uses a behavioral simulation tool without using a SPICE-like analog simulator. The behavioral model is constructed such that it is based on real circuit operation. The non-linear operation of the circuit is considered by splitting the circuit into two parts; the one for the linear part and another for the non-linear part. The non-linear function is realized by defining the formula based on the circuit operation and by applying feedback. The transient and frequency-response characteristics of the designed and fabricated current-mode buck DC-DC converter using a 0.35-um CMOS process were simulated by SPICE and the proposed program on a behavioral simulation tool, which we named NSTVR (The New Simulation Tool for Voltage Regulators). Comparing the evaluation results of the chip as well, the three kinds of results showed good agreement even though NSTVR was more than 100 times faster than SPICE in CPU time.**

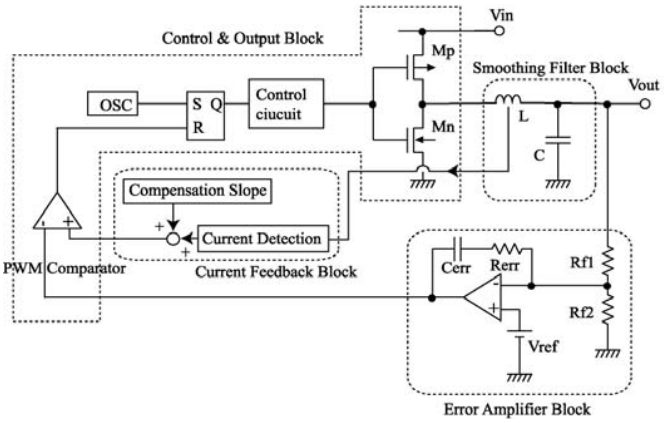

Fig. 1. Block diagram of a current-mode buck DC-DC converter.

I. Introduction

The use of DC-DC converters has become common in electronic equipments because the stable supply-voltage for circuits and LSIs must be produced by converting the voltage without consuming the power in the conversion process. In the circuit design of a DC-DC converter, the performance and characteristics are commonly evaluated by the SPICE simulation. As the DC-DC converter is inherently a negative feedback system with mixed analog and digital circuits, an analog simulator such as SPICE is typically used to simulate the loop dynamics and stability.

Figure 1, as an example, shows a block diagram of the current-mode buck DC-DC converter [1]. Blocks in Figure 1 are divided into two parts; the analog part and the digital part. The analog part consists of the smoothing filter block, the error amplifier block and the current feedback block. On the other hand, the control and output block is the digital part. Because the output voltage and current are controlled in synchronizing with the system clock which is supplied by the oscillator, voltages and currents at various nodes in the analog part change drastically at every clock cycle, although they become periodic when a DC-DC converter operates in a steady state condition.

Under these circumstances, SPICE has to simulate in very small time steps to trace the drastic value changes in the analog part and also in the digital part; as a result, the simulation time increases. In order to solve the problem, an approximated small signal model [2] was used to model the control and output block as the equivalent analog function; however, it was a linear model and couldn't handle the non-linearity of the circuit. A periodic small signal analysis was introduced [3] so that the function to perform the periodic analysis in SPICE can be utilized, acknowledging that the waveform at each node is stably periodic in the steady state of operation. Unfortunately, it didn't accelerate the transient response simulation. A method using behavioral models such in a simulator as MATLAB without using a small signal model has been proposed [4], but it has not yet been verified using actual circuits.

In this paper, a new simulation method for DC-DC converters that has faster simulation time than SPICE, that supplies simulation results as precise as those of a real chip and that is

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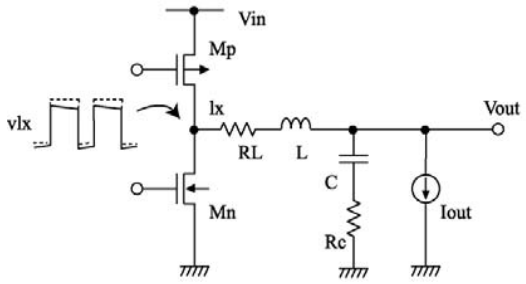
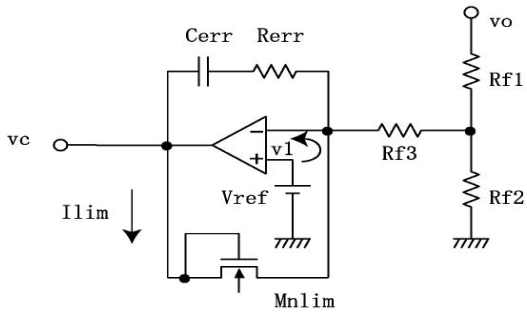
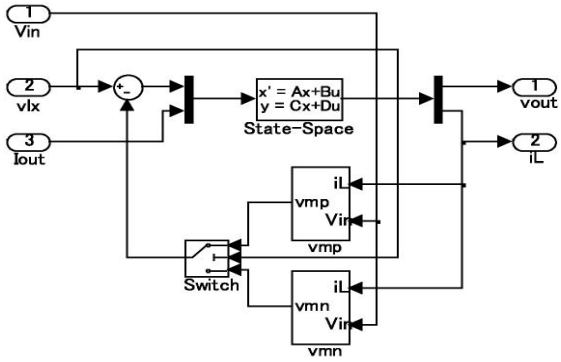


(a) Output circuit.

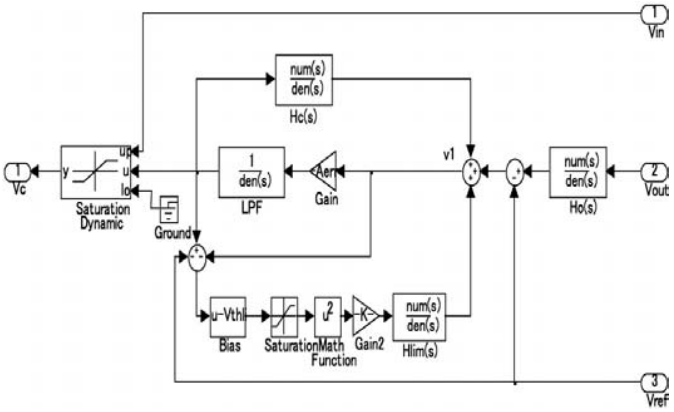


(b) Error amplifier.

Fig. 2. Circuits of two blocks in a DC-DC converter.



(a) Output circuit.



(b) Error amplifier.

Fig. 3. Modeling examples of two blocks in a DC-DC converter.

realized by behavioral simulation taking the non-linearity of circuits into account is introduced.

II. Modeling of Circuits

Strategies of modeling include the Laplace transform, state variable equations, non-linear formulae and feedback. Figure 2(a) shows the output circuit which contains output switching transistors Mp and Mn, a smoothing filter (L, C) with parasitic resistors (RL, Rc) and the current source Iout as the load. The modeling of this circuit is based on state variable equations with inductor current iL and capacitor voltage vc as variables. It is initially assumed to have ideal switching transistors and the rectangular voltage change at terminal lx in Figure 2(a). However, in fact, the voltage at lx changes as the inductor current iL changes. This phenomenon has been included in the modeling by establishing two equations, one for Mp and another for Mn, that calculate the drain-to-source voltage of transistors utilizing inductor current iL and device parameters from our 0.35-um CMOS process for coefficients of equations. Then, these equations are set to feedback to the input rectangular voltage at the lx terminal by way of a selection switch which is controlled by vlx depending on which output transistor (Mp or Mn in Figure 2(a)) becomes turn on and off as shown in Figure 3(a). Figure 3(a) is the block representation in the behavioral simulation program. We used MATLAB/Simulink as a behavioral simulation tool.

Figure 2(b) is the error amplifier. The block is modeled initially by the transfer function with an ideal operational amplifier, Vref and linear resistors and a capacitor. However, the frequency characteristics of the operational amplifier and clamping operation of M_{nlim} as a limiter need to be considered. In order to install the frequency characteristics of the operational amplifier, it is necessary to derive the equation for the difference input voltage v1, and the superposition principle was used for this purpose. As the voltage difference v1 in Figure 2(b) is expressed as superposition of influences of input signal v_o, output signal v_c, reference voltage V_{ref} and limiter current I_{lim}, therefore, the following equation holds.

$$v_1(s) = H_o(s)\, v_o(s) + H_c(s)\, v_c(s) - V_{ref} + H_{lim}(s)\, I_{lim}(s) \quad (1)$$

where $H_o(s)$, $H_c(s)$ and $H_{lim}(s)$ are transfer functions from inputs vo, vc and the limiter current Ilim of Mnlim. Now, the gain A_{err} and the frequency characteristic $1/den(s)$ of

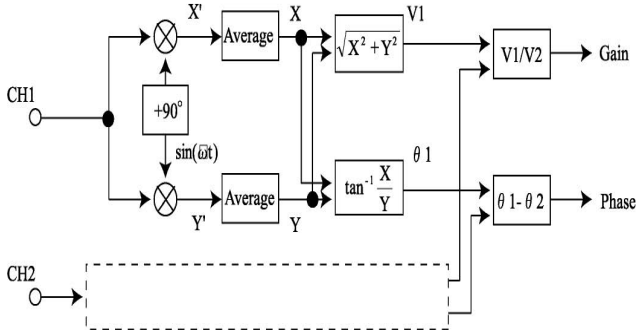


Fig. 4. Calculation of the loop gain and phase at a frequency of ω.

the operational amplifier can be defined using v_1 as the input signal and v_c as the output signal as shown in Figure 3(b).

The limiter operation is modeled by applying a current feedback. Using the transistor's current equation, Ilim(s) is calculated by using the voltage difference between v_c and v_1 across the transistor M_{nlim}, and it becomes

$$I_{lim}(s) = \frac{\beta_{lim}}{2}\{v_c(s) - (V_{ref} + v_1(s)) - V_{thlim}\}^2 \quad (2)$$

where V_{thlim} is the threshold voltage of the transistor M_{nlim}. The resultant model of the error amplifier block becomes like that shown in Figure 3(b). The non-linear element M_{nlim} is modeled as a non-linear equation in a feedback path from the output to the input of the operational amplifier.

The modeling of the circuit to obtain a compensation slope and current detection circuit has been done in a similar way considering the real circuit operation into account, where the influence of transistors' transconductances are formulated.

The digital control block is modeled using the Boolean equation and the delay function. This is based on the findings that stray capacitors of transistors don't have much influence on the time constant for waveforms at various nodes in the circuit and, therefore, on overall performance of the block; because the clock frequency is slow and it is only 5 MHz. However, the delay in the digital circuit does affect to the minimum pulse width of the control signal for output power transistors and it must be considered adequately.

III. Caluculation of the loop frequency characteristics

The method to calculate the gain and phase frequency characteristics of the total loop is described [5]. Figure 4 shows how the calculation is performed. The output signal at Vout terminal of the DC-DC converter is applied to terminal 'CH1'. The loop frequency characteristics are measured to observe the output signal at Vout terminal of the DC-DC converter by injecting the signal into the input part of the error amplifier from the outside signal source, provided that the loop is cut at the connection point between the Vout terminal and the input part of the error amplifier. To terminal 'CH2', this injected signal is applied. Then, the ratio of the signal amplitude and difference in phase are calculated using outputs from CH1 and CH2.

The principle of the detection is based on the orthogonal demodulation scheme. In the control and output block circuits, the control signal pulse to drive output power transistors becomes the PWM signal. As the spectrum of the PWM resembles to that of the frequency modulated signal, the output signal of the DC-DC converter becomes to have lots of frequency components other than the desired signal frequency component. When the input signal is multiplied by the $\sin\omega t$ and $\cos\omega t$ signals, those of which are in the same frequency as the injected or the desired frequency component, the frequency component of ω is detected after averaging as two dc components, each of which is the orthogonal component of the input signal in the frequency of ω. By using these orthogonal dc components, X and Y, the gain and phase are calculated as shown in Figure 4. As the frequency components of the input signal except for the frequency component ω are converted to other frequency components rather than dc components in above mentioned procedure, the unwanted frequency components are filtered out by taking the average and do not appear at outputs. Therefore, only the frequency components of ω is detected.

IV. Performance comparison among simulations and the measurement

In order to verify the usefulness of the proposed simulation method NSTVR, we compared our simulation results of transient and frequency characteristics with those of SPICE in Figures 5(a) and 5(b) and with those of SPICE and the measurement data of the designed and fabricated current-mode buck DC-DC converter IC using a 0.35-um CMOS process in Figure 5(c). The circuit of SPICE is the same as the circuit of the IC.

Figure 5(a) shows the simulation results of the transient response at Vout terminal when the 3-V step input voltage Vin, in Figure 1, is applied. It is simulated from time zero to 100 us in 1-ns steps by both SPICE and NSTVR (using the MATLAB/Simulink behavioral simulation tool), and the measured CPU time is listed in Table 1. Although there is a little difference between two traces in Figure 5(a), we can conclude that both traces agreed well. It was further found that the NSTVR was 144 times faster than SPICE.

Figure 5(b) also shows a comparison of the transient response simulations for the load current change. This test examines the stability and response time of the loop by giving the sudden change of the load current. The voltage at the output initially changes when the load current suddenly changes, however, it will settle back to the appropriate voltage when the loop is stable. If the phase margin of the loop is small, the transient waveform becomes ringing. If the frequency bandwidth of the loop is large enough, the transient response-time becomes short. The load current changes from 220 mA to 20 mA and vice versa in Figure 5(b), and the dynamics of a DC-DC converter is tested. It has turned out that the loop is stable and that both waveforms of the SPICE

and NSTVR are coincident with each other and NSTVR again was 98 times faster than SPICE as listed in Table 1.

Finally, figure 5(c) shows the gain and phase frequency characteristics of the total feedback loop of the DC-DC converter. These NSTVR characteristics are obtained by using the method shown in Figure 4. In addition to this, measurement data are superimposed to the simulation data. In this case, SPICE needs to repeat the transient analysis with an injected signal in a loop one at a time as the signal frequency changes. As shown in Figure 5 and Table 1, SPICE used 900 minutes only to simulate the gain and phase of the loop at four different frequencies that are denoted by X characters in Figure 5(c) while NSTVR only used 6 minutes to simulate 25 different frequencies. Data from NSTVR, SPICE, and the measurement agreed well. Moreover, NSTVR was 150 times faster than SPICE. The good agreement in phase and extremely fast simulation time indicate the effectiveness and usefulness of NSTVR.

V. Conclusions and future work

It was verified that the proposed NSVTR is 100 times faster than SPICE and as precise as the result from the real chip in a simulation of a DC-DC converter. Our future work is to further verify the effectiveness and usefulness of NSTVR by applying it to other types of DC-DC converters such as the step-up DC-DC converter and the charge pump.

TABLE I

CPU time comparison for three different simulations in Figure 5 (CPU is SUN Blade 2000 UltraSPARC III).

	Figure 5(a)	Figure 5(b)	Figure 5(c)
SPICE	3,600 sec	9,950 sec (every 10 ns)	900 min.
NSTVR	25 sec	105 sec (every 1 ns)	6 min.

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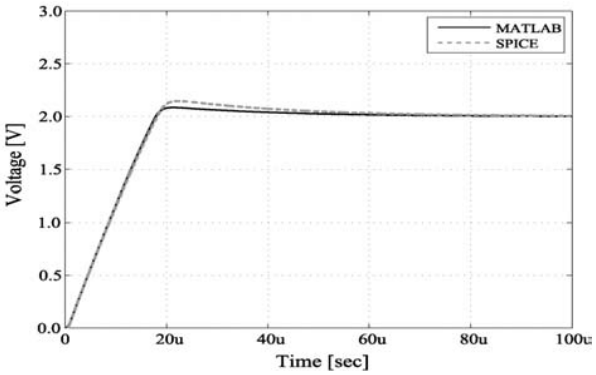
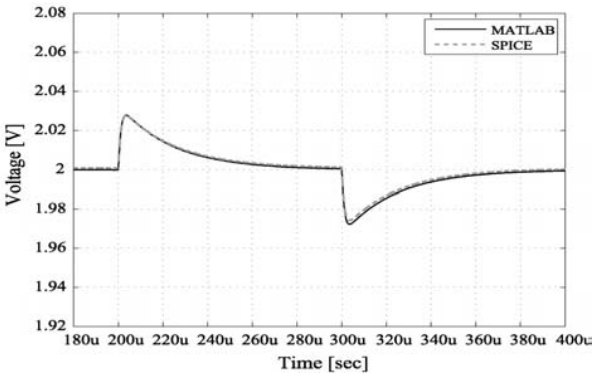
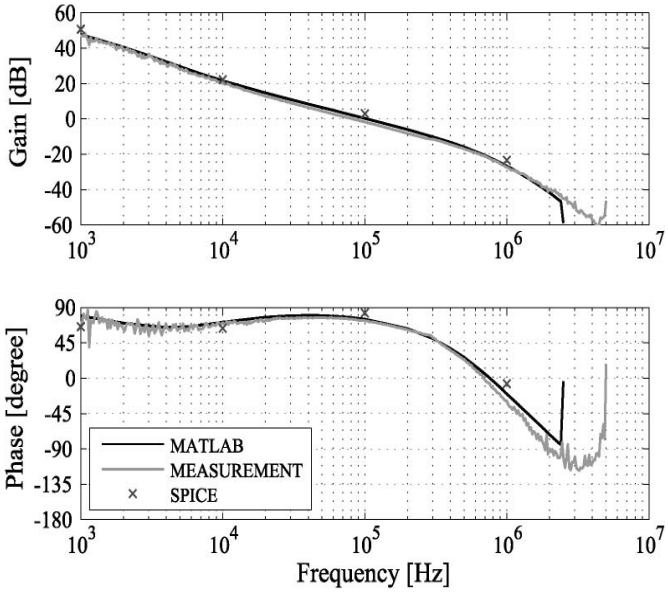


(a) Transience at Vout.



(b) Load current change.



(c) Gain and phase of the total loop (Vin=2.5V; Vout=1.5V).

Fig. 5. Performance comparison among SPICE, NSTVR and the experimental values.