IEEE Asian Solid-State Circuits Conference
November 16-18, 2009 / Taipei, Taiwan

A Method for Realizing a Fast Response Time for the Output Current Change of a MOS Current-mode Buck DC-DC Converter Which Utilizes a Quadratic and Vin-Dependent Compensation Slope

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Abstract— **In this study, a fast response time of less than 10 us has been realized for the sudden output current change between 220 mA and 20 mA of a MOS current-mode buck DC-DC converter which utilizes a quadratic and input-voltage-dependent compensation slope. By using a quadratic and input-voltage-dependent compensation slope, the frequency characteristics of the current feedback loop become constant, and the converter's overall frequency characteristics come to be determined by just adjusting the frequency characteristics in the voltage feedback loop. By changing the time constant in an error amplifier to manipulate the phase margin, the converter's output voltage change becomes small and its response time becomes fast. The test chip of a MOS current-mode buck DC-DC converter using a 0.35-um CMOS process and a 5 MHz clock realized a 40.8 mV output voltage change and a 7.2 us of the response time.**

I. Introduction

The use of DC-DC converters has become common, especially in mobile equipment, because the stable low supply-voltage for LSIs must be produced by converting the voltage from that of the lithium-ion secondary battery without consuming the power in the conversion process. As the supply currents for LSIs are frequently turned on and off to offer alternate operational capabilities between the normal mode and the stand-by mode in order to save the energy of the battery in mobile equipment, the requirement for a DC-DC converter to achieve a quick output voltage settlement both in magnitude and time when the output current suddenly changes becomes critical.

In a current-mode DC-DC converter, an inductor-current feedback loop (which will be referred to hereafter as 'a current feedback loop') is used in addition to an output-voltage feedback loop (which will be referred to hereafter as 'a voltage feedback loop') [1],[2]. The current feedback loop was introduced to extend the frequency bandwidth of a DC-DC converter without the influence of the resonance of the smoothing inductor and capacitor at the output. The response time of the output voltage when the output current suddenly changes depends on the overall loop frequency characteristics, including the series combination of the frequency characteristics of the voltage feedback loop, the current feedback loop and the load plus capacitor circuit. However, the frequency characteristics change depending on the input- and output-voltage settings in a conventional DC-DC converter, and the amount of the output voltage change and its response time deviate.

Previously, we have shown that the frequency characteristics of a current feedback loop become insensitive to the input voltage, output voltage and the output current changes of a DC-DC converter and become constant when the quadratic and input-voltage-dependent compensation slope in a current feedback loop is used [3]. This means that we can set the time constant of the total loop independently only by modifying the constant in the voltage feedback loop. In this paper, a method to render the output voltage change small and the response time short when the output current suddenly changes in a MOS current-mode buck DC-DC converter is investigated.

II. A designed DC-DC converter with a quadratic compensation slope

Figure 1 shows the circuit block diagram of a designed MOS current-mode buck DC-DC converter. It contains a voltage feedback loop and a current feedback loop. It is common for the current feedback loop to have a slope compensation circuit to enable stable operation when the turn-on interval of the power MOS transistor Mp exceeds half of the control clock interval and when the inductor current suddenly changes. We used a quadratic shape for the compensation slope [3] instead of a linear shape [4] as shown in Figure 2. In Figure 2, $T_s(= 1/f_s)$ is the clock period during which the DC-DC converter extracts the energy from the external power source V_{in} and releases it to the load R_L. V_i in Figures 1 and 2 represents the voltage that is converted from the current that is proportional to the inductor current plus the current for the slope compensation, and V_c represents the voltage at the output of the error amplifier in the voltage feedback loop. The voltage difference between V_c and V_i controls the turn-on interval of Mp through PWM comparator, R-S flip-flop and

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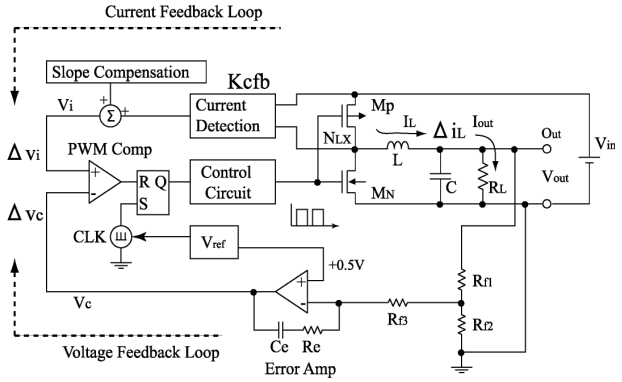


Fig. 1. Block diagram of a designed MOS current-mode buck DC-DC converter.

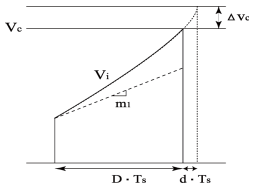


Fig. 2. Waveforms for V_i and V_c in Figure 1.

control circuit shown in Figure 1. In reality, V_i appears only when Mp turns on. Only the rising part of V_i is sufficient to produce the control signal for the output voltage.

The small signal equivalent circuit of a DC-DC converter in Figure 1 is shown in Figure 3. An error amplifier $\mathrm{A}_{err}(s)$ is in the voltage feedback loop. Z_{CR} is the impedance of a smoothing capacitor C and an equivalent load resistor R_L in parallel, which is seen at the Out terminal in Figure1, and it is the load for the output current of the current feedback loop. T_{cm} represents the transfer function from the difference voltage $\Delta v_f = \Delta v_c - \Delta v_i$ to the duty ratio Δd. T_{ps} is the voltage conversion ratio from the duty ratio to the output voltage at the terminal N_{LX}. Y_{LCR} is the admittance of the output smoothing circuit including an external inductor L, a capacitor C and the load R_L in Figure 1. K_{cfb} is the current to voltage conversion ratio from the inductor current I_L to V_i without the slope compensation. $\mathrm{H}_e(s)$ is the sampling function [4].

With the slope compensation, the small signal transfer function of the current feedback loop becomes similar to that of the second-order low-pass filter as follows,

$$\frac{\Delta i_L}{\Delta v_c} = \frac{1}{K_{cfb}} \cdot \frac{1}{1 + \frac{2s}{\omega_n}\zeta + \frac{s^2}{{\omega_n}^2}} \tag{1}$$

where $\omega_n = \pi f_s$ is the natural frequency and it is at half the clock frequency. The damping factor when the quadratic slope is used is calculated as in [3],

$$\zeta = \frac{\pi L}{2V_{in}K_{cfb}}\left(m_1 + 2{m_c}' DT_s\right) - \frac{\pi}{4} \tag{2}$$

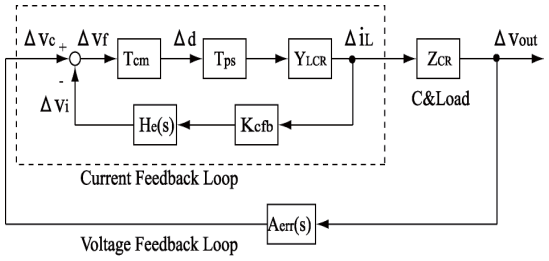


Fig. 3. The small signal equivalent circuit of a DC-DC converter in Fig. 1.

where T_s is the clock period, m_1 is the slope which is shown by the dotted line in Figure 2 and is proportional to the inductor current, and ${m_c}'$ is the coefficient of the quadratic slope. Here, m_1 is

$$m_1 = \frac{(V_{in} - V_{out})\, K_{cfb}}{L} \tag{3}$$

We choose the damping factor ζ to be greater than 1/2 so that a second-order system such as a low-pass filter does not have a gain peak at all frequencies. Then ${m_c}'$ becomes

$${m_c}' \geq \frac{V_{in}K_{cfb}f_s}{2L}\left\{1 + \left(\frac{1}{\pi} - \frac{1}{2}\right)\frac{1}{D}\right\} \tag{4}$$

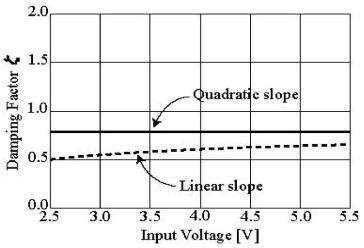
The right-hand side of equation (4) is at a maximum when D is 1; therefore,

$${m_c}' = \frac{V_{in}K_{cfb}f_s}{2L} \tag{5}$$

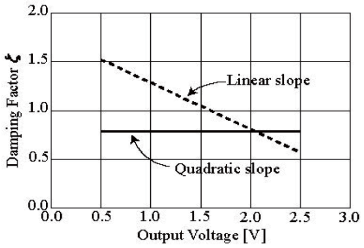
is chosen as the appropriate value. Of course, equation (5) satisfies the criteria of equation (4). Then, the ζ value becomes $\pi/4$, i.e., constant, and equation (1) also becomes unaltered. This means that the frequency characteristics of the current feedback loop become independent of V_{out}. However, it is obvious from eq. (5) that ${m_c}'$ must depend on V_{in}.

The linear Vin dependency of ${m_c}'$ in eq. (5) is realized in the current detection and the slope compensation circuit by introducing a resistor which reveals the input voltage dependency. This resistor is realized by a PMOS transistor which is driven in a triode region by having its source and gate terminals connected to the V_{in} and ground, respectively [3].

The effect of making the compensation slope quadratic and Vin-dependent enables the damping factor of the current feedback loop to remain constant for both Vin and Vout changes as shown in Figure 4. When a linear slope is used, the damping factor ζ changes when the input and output voltages are chosen differently. This means that the frequency characteristics change depending on the input- and output-voltage settings. In contrast to this, when the input-voltage-dependent quadratic slope is used, the damping factor becomes fixed at $\pi/4$. Completely unaltered frequency characteristics are expected.

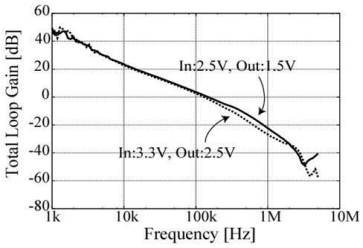


(a) Vin dependency.

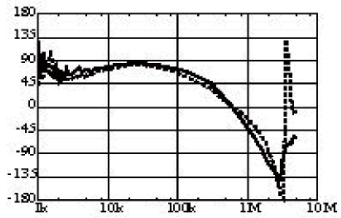


(b) Vout dependency.

Fig. 4. The effect of the quadratic and Vin-dependent slopes.



(a) Gain characteristics: 0 dB bandwidths are 150 kHz and 136 kHz.



(b) Phase characteristics: Phase margins are 66° and 59°.

Fig. 5. Frequency characteristics of the total feedback loop with bandwidths of 150 kHz and 130 KHz.

III. Achieving unaltered frequency characteristics

In order to see the effect of using the quadratic and Vin-dependent compensation slope, a test IC was fabricated using a 0.35 um CMOS process. Figure 5 shows the frequency characteristics of the total feedback loop of a DC-DC converter at two different input and output voltage settings. The clock frequency is 5 MHz. The frequency bandwidth is chosen to be approximately 140 kHz by adjusting the parameter R_e in the error amplifier for the two settings in Figure 5.

Figure 5(a) shows the gain frequency characteristics, and Figure 5(b) shows the phase frequency characteristics. In this measurement, the input signal is injected from the upper side terminal of R_{f1} in Figure 1 by cutting away the ac connection from the Out terminal, though the dc path remains, and the output signal is detected at the Out terminal [5]. In each figure, (a) and (b), two curves are drawn. One is a curve with a 2.5-V input voltage and a 1.5-V output voltage, i.e., a duty ratio of 60 %. The other curve has a 3.3-V input voltage and a 2.5-V output voltage for a duty ratio of 75 %. Figure 5 tells that the frequency bandwidths are 150 kHz and 136 kHz and the phase margins are 66 degrees and 59 degrees, respectively, for two different input and output voltage settings. No significant difference can be seen, even in the curves of the phase frequency characteristics. It is obvious that constant frequency characteristics were obtained without depending on the input and output voltages.

IV. Reducing response time by adjusting the time constant in the voltage feedback loop

The frequency characteristics of the total feedback loop consist of a combination of those of a voltage feedback loop, a current feedback loop and the impedance Z_{CR} in Figure 3 in series. The frequency characteristics of the current feedback loop become constant, and the frequency characteristics of the total feedback loop of a DC-DC converter can be determined by choosing the time constant in the voltage feedback loop and Z_{CR}. Figure 6 shows the circuit of the voltage feedback loop. The output current, which is assumed to flow in the load resistor R_L, is 100 mA. With settings of V_{in}=3.3 V and V_{out}=2.5 V, R_{f1}, R_{f2} and R_{f3} are set at 40 kΩ, 10 kΩ and 2 kΩ, respectively. When R_e=250 kΩ and C_e=100 pF, the frequency bandwidth of the total feedback loop becomes approximately 70 kHz, and the frequency characteristics (transfer function) become like curve I, shown as a solid line in Figure 7. Curve I has three poles and one left-half plane zero. The first pole and the zero come from the time constant in an error amplifier, and their location in frequencies can be modified. The second pole is produced by Z_{CR} which consists of C and R_L in Figure 6, and the third pole is from the error amplifier itself.

By changing the value of R_e from 250 kΩ to 450 kΩ, we can extend the frequency bandwidth from 70 kHz to 136 kHz and increase the voltage gain in the intermediate frequency range, as in curve II, which is indicated by the chain line in Figure 7. A large frequency bandwidth is expected to realize a

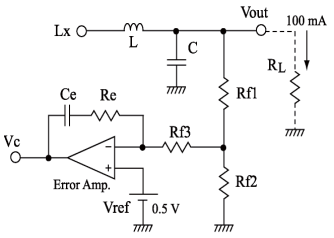


Fig. 6. The circuit configuration in the voltage feedback loop.

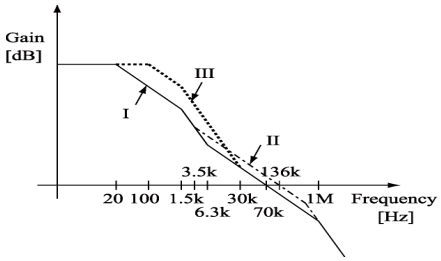
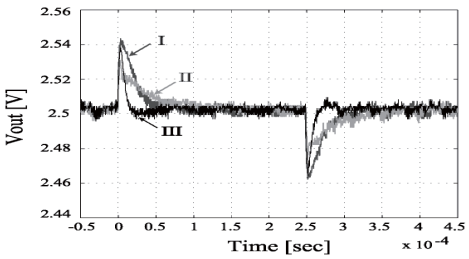
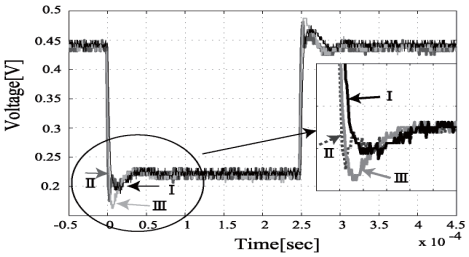


Fig. 7. Frequency characteristics of the total feedback loop for various configurations in an error amplifier.



(a) The transient response at the DC-DC output.



(b) The transient response at the error amplifier output.

Fig. 8. The transient when the output current changes between 220 mA and 20 mA.

fast response time for any sudden current change at the output, but no distinct difference was seen in the transient response in the cases for curves I and II. We found that the waveform overshoot at the output of the error amplifier did influence the transient response. The duty-ratio, that is, the turn-on time of an output power transistor, changes due to the overshoot, and the output voltage of a DC-DC converter is accelerated to settle down. Therefore, the first pole and zero are moved to the high frequency, as shown in line III in Figure 7, so that the phase margin in the voltage feedback loop becomes a little smaller. As a result, the overshoot appears at the output of the error amplifier. In this design, reducing the phase margin has been realized by choosing a C_e value of 22 pF and moving the first pole to 100 Hz. The first pole is expressed as,

$$z_{p1} = -\frac{1}{C_e A_{err}\{R_{f3} + (R_{f1}//R_{f2})\}} \tag{6}$$

Where A_{err} is the low frequency voltage gain of an error amplifiler. The frequency bandwidth of the total loop remains the same at 70 kHz as curve I.

Figure 8 shows evidence of response time improvement. The response curves I, II and III in Figure 8 correspond to frequency characteristics I, II and III in Figure 7, respectively. In Figure 8(a), a transient response at the output is shown when the output current changes alternately from 220 mA to 20 mA and vice versa. The input and output voltages of the DC-DC converter are set to 3.3 V and 2.5 V, respectively. We can see the improvement in response time in case III to 7.2 us and 7.0 us, corresponding to the positive and negative voltage changes, respectively. Figure 8(b) shows waveforms at the output of the error amplifier at the time when the output current changes. In case III, the overshoot was large, as expected. Therefore, a fast transient response was obtained.

V. Conclusion

In the MOS current-mode buck DC-DC converter, the use of the quadratic and input-voltage-dependent slope for a current feedback loop made the frequency characteristics of the current feedback loop constant. The frequency characteristics of the total loop are independently adjusted by the pole and zero produced in an error amplifier. Decreasing the phase margin at intermediate frequencies was effective for achieving a fast response time in the case of a sudden output current change.

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