A MOS Current-mode Buck DC-DC Converter with a 240-kHz Loop Bandwidth and Unaltered Frequency Characteristics using a Quadratic and Input-voltage-dependent Compensation Slope

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***Abstract*— In this study, we verified that a quadratic slope was the best-fit compensation slope for the current feedback loop of a current-mode DC-DC converter by considering the stability of the inductor current when the current disturbance was applied. We also verified that the introduction of the input voltage dependency to the quadratic slope enabled the frequency characteristics of the current feedback loop to remain completely constant without depending on the input and output voltage change of a DC-DC converter. The test chip of a MOS current-mode buck DC-DC converter using a 0.35-μm CMOS process and a 5-MHz clock realized two loop frequency bandwidths of 130 kHz and 240 kHz and was operated in two different input and output voltage settings for each frequency bandwidth. As a result, the unaltered gain and phase frequency characteristics were obtained for two different settings in each frequency bandwidth.**

I. Introduction

In a DC-DC converter, an inductor-current feedback loop (which will be referred to hereafter as 'a current feedback loop') and an output-voltage feedback loop (which will be referred to hereafter as 'a voltage feedback loop') are used, with the result that the voltage change and the current change at the output terminal are quickly regulated [1],[2]. The current feedback loop was introduced to extend the frequency bandwidth of a DC-DC converter without the influence of the resonance of the smoothing inductor and capacitor at the output. When a DC-DC converter is used, however, the input voltage, output voltage and output current change, depending on the converter's usage, and the stability, i.e., the frequency characteristic of the current feedback loop, changes, making it necessary to adjust the amount of feedback to accommodate the change in each application. This situation should be avoided if possible. For the frequency characteristics of a current feedback loop to be insensitive to the input voltage, output voltage and the output current changes of a DC-DC converter, the use of the quadratic slope has been proposed [3], but it is not clear whether the quadratic slope is the best-fit compensation slope. Moreover, the influence of the input voltage dependency on the quadratic slope has not been clarified. We propose the use of the quadratic slope with input-voltage dependency. Our results show that a wide frequency bandwidth and unaltered frequency characteristics of a MOS current-mode buck DC-DC converter can be obtained.

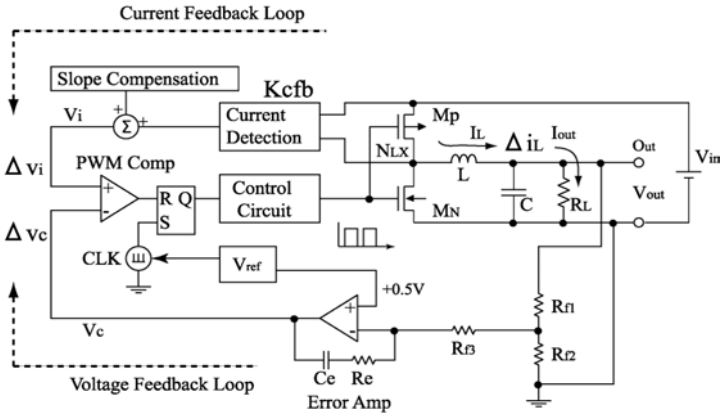

Fig. 1. Block diagram of a MOS current-mode buck DC-DC converter.

II. The best-fit slope for the current feedback loop

Figure 1 shows the block diagram of a MOS current-mode buck DC-DC converter. It is common for the current feedback loop to have a slope compensation circuit to enable stable operation when the turn-on interval of the power MOS transistor Mp exceeds half of the control clock interval and when the inductor current suddenly changes. Figure 2(a) shows the conceptual waveforms of Vi and Vc in Figure 1 of the conventional DC-DC converter, which utilizes a linear compensation slope [4]. Vi is the voltage that is converted from the current which is proportional to the inductor current. Vc is the sum of the voltage at the output of the error amplifier in the voltage feedback loop and the voltage converted from the current for the slope compensation. The voltage difference between Vc and Vi controls the turn-on interval of Mp. In reality, only the rising part of Vi is sufficient to produce the

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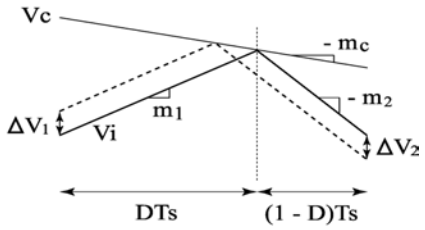
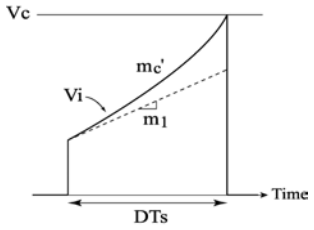


(a) Conceptual Vi and Vc in Fig. 1.



(b) Desired waveforms for Vi and Vc.

Fig. 2. Waveforms at input terminals of the PWM comparator.

control signal for the output voltage, and the I/V converted voltage of a linear compensation slope current is added to Vi instead of Vc, although the linear and negative slope was included in Vc in Figure 2(a).

Consider a step current change in an inductor. The change is transferred to the control voltage Vi, as seen in Figure 2(a). For a sudden inductor current change to be settled, ΔV_2 must be smaller than ΔV_1. This equals

$$\frac{\Delta V_2}{\Delta V_1} = -\frac{m_2 - m_c}{m_1 + m_c}, and \mid \Delta V_2 \mid < \mid \Delta V_1 \mid \tag{1}$$

and the condition for m_c becomes

$$m_c > \frac{(2D-1)\,V_{in}}{2L} K_{cfb} \tag{2}$$

Here, m_1, m_2 and m_c are the slope coefficients of Vi and Vc, as seen in Figure 2(a). K_{cfb} is the I/V conversion coefficient of the current detection circuit block depicted in Figure 1 and is constant once it is designed; D (=V_{out}/V_{in}) is the duty factor that shows the turn-on time of a transistor Mp out of one clock period of the control; and L is the inductance value of an external inductor in Figure 1. When Vin is constant, Equation (2) means that the compensation slope m_c should increase linearly as D increases. This results in the waveform for the compensation slope becoming quadratic, as shown in Figure 2(b), where the quadratic slope is added to the I/V converted voltage from the current that is proportional to the inductor current. When Vi reaches Vc, the output of the PWM comparator in Figure 1 becomes high, and this turns off the power transistor Mp.

III. The use of the quadratic slope

With the slope compensation, the small signal transfer function of the current feedback loop becomes similar to that of the second-order low-pass filter, as follows:

$$\frac{\Delta i_L}{\Delta v_c} = \frac{1}{K_{cfb}} \cdot \frac{1}{1 + \frac{2s}{\omega_n}\zeta + \frac{s^2}{{\omega_n}^2}} \tag{3}$$

where $\omega_n = \pi f_s$ is the natural frequency and it is at half the clock frequency. When the quadratic slope is used, the damping factor ζ is calculated as follows:

$$\zeta = \frac{\pi L}{2V_{in}K_{cfb}} \left(m_1 + 2{m_c}' DT_s\right) - \frac{\pi}{4} \tag{4}$$

where T_s is the clock period, m_1 is the slope shown by the dotted line in Figure 2(b) and is proportional to the inductor current, and ${m_c}'$ is the coefficient of the quadratic slope. Here, m_1 is determined as follows:

$$m_1 = \frac{(V_{in} - V_{out})\,K_{cfb}}{L} \tag{5}$$

We chose the damping factor ζ to be greater than 1/2 so that a second-order system such as a low-pass filter would not have the gain peak at all frequencies. In that case, ${m_c}'$ is determined as follows:

$${m_c}' \geq \frac{V_{in}K_{cfb}f_s}{2L} \left\{1 + \left(\frac{1}{\pi} - \frac{1}{2}\right)\frac{1}{D}\right\} \tag{6}$$

The right-hand side of equation (6) is at a maximum when D is 1, and therefore the following is chosen as the appropriate value:

$${m_c}' = \frac{V_{in}K_{cfb}f_s}{2L} \tag{7}$$

Of course, equation (7) satisfies the criteria of equation (6). Then, the ζ value becomes $\pi/4$, i.e., constant. This means that the frequency characteristics of the current feedback loop become independent of Vout. However, it is obvious from equation (7) that ${m_c}'$ needs to depend on Vin.

IV. Vin-dependent slope generation and its circuit

The Vin dependency of ${m_c}'$ in equation (7) is realized in the current detection and the slope compensation circuit, as shown in Figure 3. Mp and Mn in Figure 3 represent the output power transistors of a DC-DC converter. When Mp turns on to charge an external inductor L, SW1 turns on while SW2 turns off, and the voltage at terminal NLx is applied to the positive input terminal of operational amplifier 'op1'. The voltage at the negative input terminal of 'op1' becomes equal to the voltage at the positive input terminal due to the feedback operation performed by 'op1' and Mc2. Because the drain voltages of Mp and Mc1 are equal, and the gate of Mp is tied to the ground when Mp turns on, the inductor current that flows in Mp is mirrored to the current in Mc1 by the ratio of the transistor size. The current in Mc1 also flows in Rcd, and the replica voltage Vi, which is proportional to the inductor current, is obtained across Rcd.

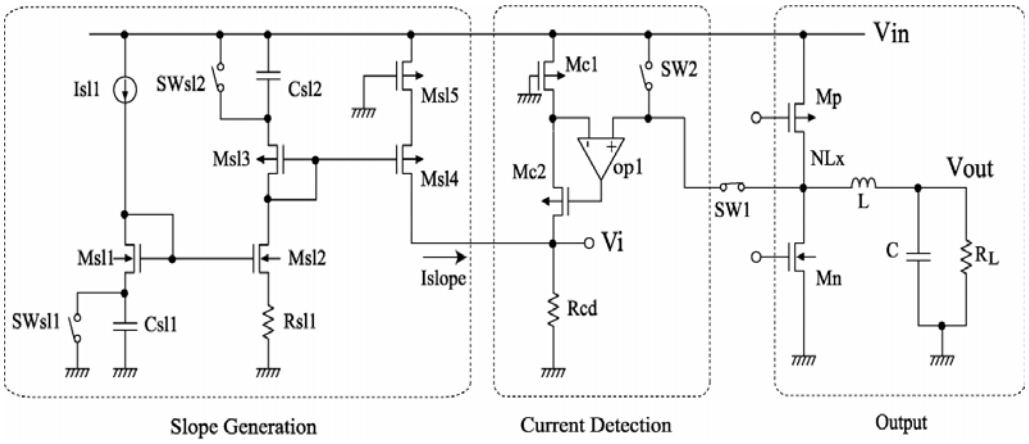


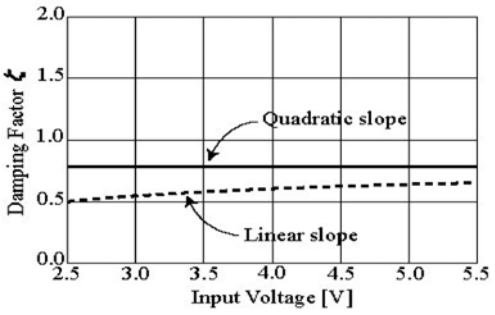
Fig. 3. A current detection and compensation slope generation circuit.

The quadratic compensation slope is generated by integrating a constant current twice using capacitors, as shown in Figure 3. The current Isl1 is constant, and the voltage across Csl1 increases with time when the switch SWsl1 turns off in synchronization with the turning on of the power transistor Mp. The voltage across Csl1 is copied to the voltage across Rsl1, and a current that increases linearly with time flows in Rsl1. The current in Rsl1 flows in Csl2, and the voltage across Csl2 becomes quadratic with time due to the time integration of the linearly increasing current in time by Csl2. The turning off of the switch SWsl2 is also synchronized with the turning on of the power transistor Mp. Again, the voltage across Csl2 is copied to the voltage across Msl5. As Msl5 is like a linear resistor, because it is driven in a triode region by its gate terminal being connected to the ground, the current Islope becomes quadratic with time and is converted to the voltage by Rcd through Msl4. The resultant quadratic slope voltage together with the voltage that is proportional to the inductor current becomes like that shown in Figure 2(b). The resistor value RMsl5 seen from the drain terminal of Msl5 in a triode region is approximated as follows:

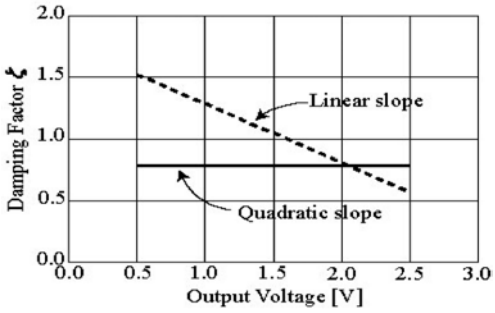
$$R_{Msl5} \approx \frac{1}{\beta\left(V_{GSMsl5} - V_{th}\right)} \approx \frac{1}{\beta V_{in}} \tag{8}$$

where β is the transconductance coefficient of Msl5. Assuming Vth is small, $(V_{GSMsl5} - V_{th})$ is approximated to Vin because the gate of Msl5 is grounded. As the Islope is determined by the division of the quadratic voltage change with time by the resistor in equation (8), we note that the coefficient of the Islope and, therefore, the voltage across Rcd due to the Islope becomes proportional to Vin. In this way, $m_c{}'$ in equation (7) becomes linearly dependent on Vin.

Making the compensation slope quadratic and Vin-dependent enables the damping factor in equation (3) to remain constant for both Vin and Vout changes, as shown in Figure 4. When the linear slope is used, the damping factor ζ changes when the input and output voltages are chosen differently. As the damping factor governs the frequency characteristics of the current feedback loop, the frequency characteristics change depending on the input and output voltage settlement. In contrast to this, when the input-voltage-dependent quadratic slope is used, the damping factor becomes fixed at $\pi/4$. Completely unaltered frequency characteristics are expected.



(a) Vin dependency.

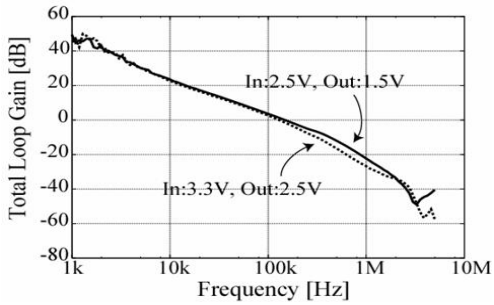


(b) Vout dependency.

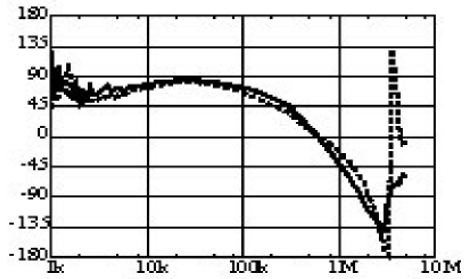
Fig. 4. The effect of the quadratic and Vin-dependent slope.

V. Experimental results

To verify the effect of the quadratic and Vin-dependent compensation slope, we fabricated a test IC using a 0.35-μm

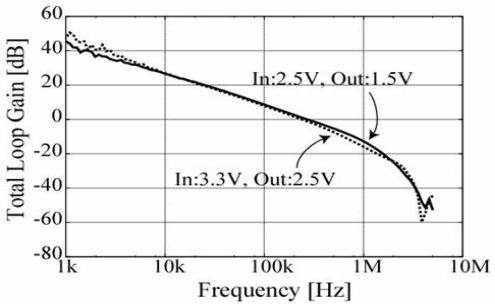


(a) Gain characteristics: The 0-dB bandwidths are at 150 kHz and 130 kHz.

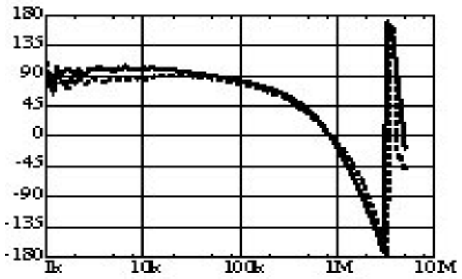


(b) Phase characteristics: The phase margins are 66° and 59°.

Fig. 5. Frequency characteristics of the total feedback loop with bandwidths of 150 kHz and 130 KHz.



(a) Gain characteristics: The 0-dB bandwidths are at 270 kHz and 240 kHz.



(b) Phase characteristics: The phase margins are 65° and 62°.

Fig. 6. Frequency characteristics of the total feedback loop with bandwidths of 270 kHz and 240 kHz.

CMOS process. Figure 5 and Figure 6 show the frequency characteristics of the total feedback loop in two different input and output voltage settings. The clock frequency was 5 MHz. Although the frequency characteristics of the current feedback loop were fixed, the frequency characteristics of the total feedback loop, which consisted of the combination of the frequency characteristics of the voltage feedback loop, the current feedback loop and the C and R_L together at the output in Figure 1, could be adjusted by using parameters C_e and R_e of the error amplifier in the voltage feedback loop and the external capacitor C at the output.

Figure 5 shows the gain and phase frequency characteristics when the frequency bandwidth is chosen to be approximately 140 kHz. Figure 6 shows the gain and phase frequency characteristics when the frequency bandwidth is chosen to be approximately 250 kHz. In each figure, (a) and (b), two curves are drawn. One is a curve with a 2.5-V input voltage and a 1.5-V output voltage, i.e., a duty ratio of 60%. The other curve has a 3.3-V input voltage and a 2.5-V output voltage with a duty ratio of 75%. With the two different input and output voltage settings described above, the frequency bandwidths were 150 KHz and 130 kHz and the phase margins were 66° and 59°, respectively, in the case shown in Figure 5. In Figure 6, the frequency bandwidths were increased to 270 kHz and 240 kHz with phase margins of 65° and 62°, respectively. In both cases in Figures 5 and 6, no significant difference can be seen, even in curves of phase frequency characteristics for two different input and output voltage settings. It is obvious that constant frequency characteristics were obtained without depending on the input and output voltages.

VI. Conclusion

The use of the quadratic and input-voltage-dependent slope for a current feedback loop of the MOS current-mode buck DC-DC converter realized a wide loop bandwidth and completely unaltered frequency characteristics without depending on the input and output voltage changes.

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