The Influence of Dummy Fills on an On-chip Spiral Inductor and their Optimized Placement Scheme

Tatsuya Ogino[1], Yasuhiro Sugimoto[2]
[1]Graduate school of E., E., and C. Engineering, Chuo University, Japan
[2]Department of E., E., and C. Engineering, Chuo University, Japan
[1]ogi@sugi.elect.chuo-u.ac.jp

Introduction

On-chip spiral inductors are widely used in radio-frequency circuits. In the advanced LSI process, however, the automatic placement of metal dummy fills has become standardized [1]. The question arises as to whether or not metal dummy fills spoil the quality of an on-chip spiral inductor because they are placed inside, outside, and even beneath the inductor wires.

It has been revealed that the eddy-current losses that occur on metal dummy fills can be minimized when the metal dummy fill is small [2], and that the placement of metals beneath the inductor causes an increase in the stray capacitance between the inductor wires and the silicon substrate [3]. This increase results in a deterioration of the self-resonant frequency. In addition, we have observed that dummy fills placed in the vicinity of inductor wires still induce eddy-current loss even if the dummy-fill size is small. The induction occurs because of the strong magnetic field which vertically penetrates the dummy fills nearby the inductor wires. Considering these conditions, we propose herein a new dummy fill placement scheme by taking into account the influence of eddy-current losses, the stray capacitances, and the magnetic field strength. The proposed placement scheme was confirmed by measurement data of fabricated inductors using a 0.18-um CMOS process with 5 metal layers.

Magnetic field strength around inductor wires

We recognized that the magnetic field in the vicinity of the inductor wires is stronger than that in other places. Figure 1 shows the EM (electro-magnetic) simulated magnetic field vectors around wires at one side in a rectangular shape of a two-turn on-chip spiral inductor. The signal current flows from backward to forward in the figure. We modeled an inductor structure in the EM simulation that is surrounded by silicon dioxide between the silicon substrate and the air. It can be understood from Fig. 1 that the eddy current loss in the dummy fills underneath the inductor wires is negligible because the arrows in the figure become parallel and the area on the dummy fill that vertically faces the magnetic field is very small. It can also be seen that arrows in the vicinity of the inductor wires become fat in width and long in length, indicating that the magnetic field is strong in such areas.

That is the reason why we needed to know the magnetic field strength at various places on the same plane as the inductor. There were no dummy fills in this case. Figure 2 shows the examined results of the magnetic field strength along a line parallel to the inductor wires in a rectangular shape. The inductor has an empty area at its center and outside the inductor wires and is 170×170 um^2 in size. Two inductor wires are placed a distance of 58.5 um to 85 um from the center of the inductor. From Fig. 2, it can be concluded that magnetic field in the vicinity of the inductor wires is very strong. In particular, the magnetic field inside the spiral inductor is stronger than that outside the inductor.

A proposed dummy fill placement scheme

Considering that the size of the dummy fills should be minimized in order to reduce the eddy-current loss, that dummy fills underneath the inductor wires should be removed in order

978-1-4244-2642-3/08/$25.00 ©2008 IEEE

to avoid an increase in capacitance between the inductor wires and the silicon substrate, and that the magnetic field is strong in the vicinity of the inductor wires, we propose that dummy fills be placed as shown in Fig. 3(b). Figure 3(a) and 3(b) shows two layout patterns. Figure 3(a) is the layout pattern that maintains the design rule of the 0.18-um CMOS process except that the dummy-fill size is shrunken from 10 um to 2 um. It uses 2×2 um^2 dummy fills with a separation distance of 2 um, with the fills being placed inside, outside, and even beneath the inductor wires. For the dummy fills on the same metal layer as the inductor wires, a vacant space of 10 um around the inductor wires is preserved. The fill ratio remains 25 %. In contrast, the layout pattern in Fig. 3(b) has a forbidden area for the placement of all layers of dummy fills from 15 um inside to 10 um outside of the inductor wires. The size of the dummy fills is 2×2 um^2, and the distance between the dummy fills is also 2 um. The pattern shown in Fig. 3(b) is our proposed one and, in this paper, the performance as an inductor is compared with the inductor shown in Fig. 3(a).

Q-value measurement result

The on-chip spiral inductors shown in Fig. 3(a) and 3(b) were fabricated using the standard 0.18-um CMOS process. Spiral inductors were formed by using the 5th metal layer which is located 7-um away from the silicon substrate. The 4th metal layer was used as the under path. The thicknesses of the metal layers are 0.99 um and 0.57 um for the 5th and the 4th layers, respectively. The spiral inductor had two turns, and its size and inductance were 170×170 um^2 and 1 nH, respectively. The metal line width was 12 um, and the distance between the winding lines was 2.5 um. An additional inductor without any dummy fills was fabricated for the purpose of comparison.

Figure 4 shows the measurement results for the frequency characteristics of the Q value from 100 MHz to 20 GHz. The curve “Normal” in Fig. 4 shows the Q value of an on-chip spiral inductor without metal dummy fills, the curve “Full” complete with dummy fills as shown in Fig. 3(a), and the curve “15u” with the forbidden area of dummy fills as shown in Fig. 3(b). Curves from “Normal” and “15u” are similar to each other. No quality degradation for the proposed placement scheme in Fig. 3(b) is seen at any frequency. The peak Q value of “15u” is close to that of “Normal,” which verifies the effect of removing the dummy fills in the vicinity of the inductor wires. In contrast, a prominent Q value degradation at frequencies greater than several GHz occurs in the case “Full”. This degradation is caused by the decrease in the self-resonant frequency, primarily due to the existence of capacitance underneath the inductor wires.

Parameter values of an equivalent circuit model

The measured S-parameters were rearranged to convert to the parameter values of the equivalent pi circuit model [4]. Figure 5 shows the frequency characteristics of each parameter value in the pi circuit model.

Rs and Ls in Fig. 5(a) and 5(b) are the equivalent series resistance and the inductance with inclusion of the parasitic capacitances, respectively, of a spiral inductor. The 2×2 um^2 size of the dummy fills is already small enough to not create a big difference in the eddy-current loss. However, a small difference between the curve “Full” and curves “Normal” and “15u” can be seen in the graph of the series resistance. This difference probably stems from the difference in the total eddy-current loss depending on the placement of the dummy fills. The influence of the magnetic field strength in the vicinity of the inductor wires is not clear for this level (5 or 6) of Q value.

Cp and Rp in Fig. 5(c) and 5(d) represent the effective capacitance and the resistance, respectively, between the spiral inductor and the silicon substrate, including the substrate capacitance and the substrate loss. An increase in Cp for "Full" can be clearly seen in Fig. 5(c). The percentage of the area where the metal dummy fills are placed is 25 % for "Full," and in Fig. 5 an increase in Cp of approximately 25 % is seen as well as a decrease in Rp. It is evident that the increase in Cp is due to the existence of dummy-fills underneath the inductor wires. These dummy fills should therefore be removed.

Conclusion

A new dummy fill placement scheme which has a forbidden area in the vicinity of and underneath the inductor wires of an on-chip spiral inductor is proposed. Experimental results showed no degradation in either the Q value or the resonant frequency for the proposed scheme.

References

[1]B.E.Stine et.al., "The Physical and Electrical Effects of Metal-Fill Patterning Practices for Oxide Chemical-Mechanical Polishing Processes," *IEEE Trans. Electron Devices,* vol.45, no.3, pp.665-679, March 1998.

[2] F.Zhang, C.F.Chu, and P.Kinget, "Voltage-Controlled Oscillator in the Coil," *IEEE 2005 Custom Integrated Circuits Conference,* Paper no.17-6, pp.587-590, September 2005.

[3] L.Nan et.al., "Experimental Characterization of the Effect of Metal Dummy Fills on Spiral Inductors," *IEEE 2007 Radio Frequency Integrated Circuit Symposium,* pp.307-310, June 2007.

[4] C.P.Yue, and S.S.Wong, "Physical Modeling of Spiral Inductors on Silicon," *IEEE Trans. Electron Devices,* vol.47, no.3, pp.560-568, March 2000.

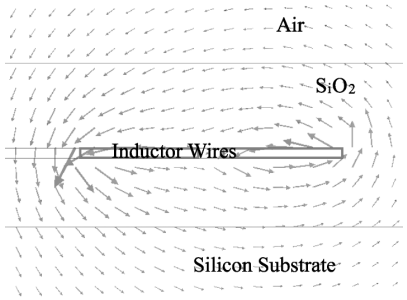

Figure 1. Direction and strength of the magnetic field vector around the inductor wires.

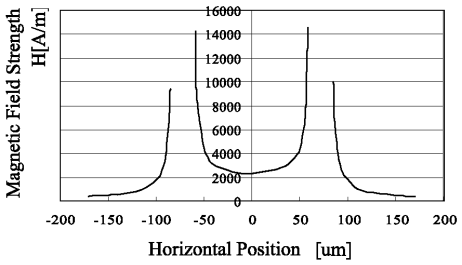

Figure 2. Magnetic field strength around the inductor.

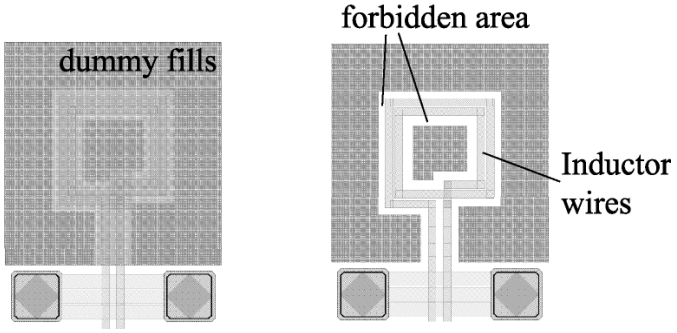

Figure 3. Layout patterns of examined on-chip spiral inductors.

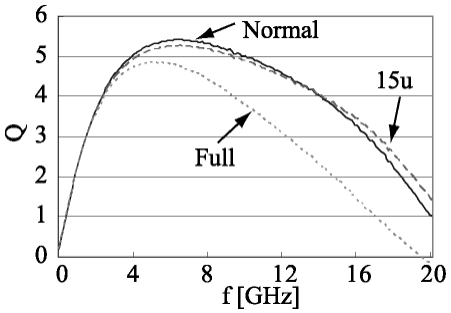

Figure 4. Measured Q-value frequency characteristics with and without metal dummy fills.

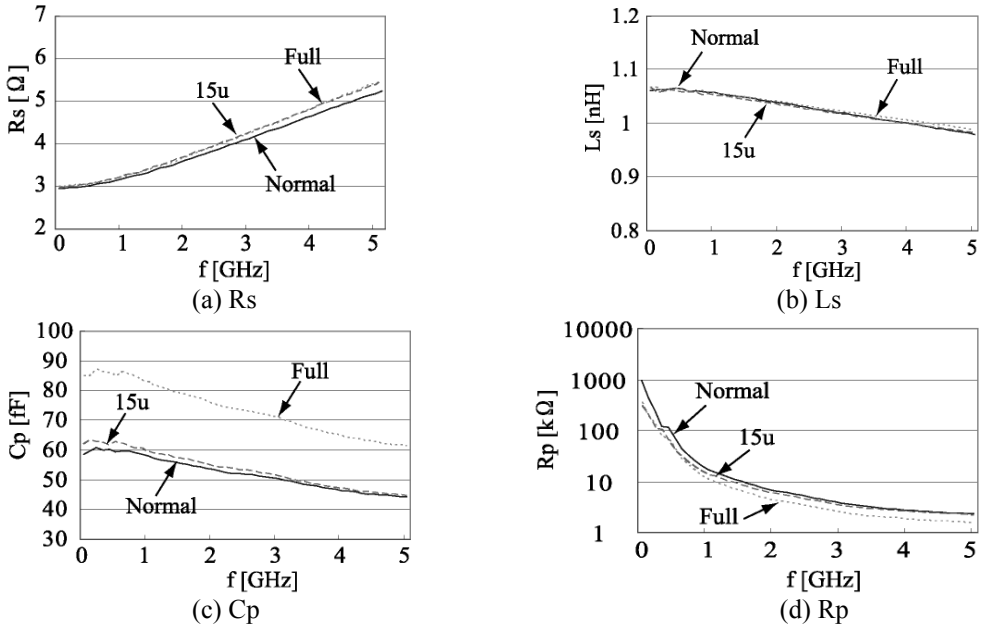

Figure 5. Measured frequency characteristics of parameters in the equivalent pi circuit model with and without metal dummy fills.