A Current-mode ADC with Current Exchanging and Averaging Capabilities by Switching the Currents and Calculating Data in the Digital Domain

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Abstract-A 2 V, 25 MS/s, current-mode and pipelined analog-to-digital converter (ADC) which realizes a 1.5-bit bit-block architecture and uses a front-end current-mode sample-and-hold (S/H) circuit is described. In order to obtain the precise output current without suffering from poor current mismatch in a bit-block, the input and output currents in a current-mirror circuit are exchanged at every clock period. This produces signal currents at the output of a bit-block with positive and negative mismatch errors in turn. Since the analog-to-digital (A-D) converted digital codes of a bit-block contain these positive and negative mismatch errors, the errors are canceled out by taking the average of the consecutive digital codes at the output part of the ADC. A current-mode ADC using this proposed scheme has been fabricated by using 0.25 um CMOS devices. The results show that the effective number of bits (ENOB) is 7.6, that the spurious-free dynamic range (SFDR) is 48 dB, with a 20 MHz clock from a 2 V supply voltage.

I. INTRODUCTION

The growing popularity of battery operated mobile devices requires the development of more low-voltage and low-power analog-to-digital converters (ADCs). This trend is followed by device scaling in the LSI process, since small size transistors have low breakdown voltage.

Current-mode circuits are considered suitable to realize low-voltage and low-power circuits [1]. As current signal processing requires high impedance for the current signal source and low impedance for the load, every node impedance in a current-mode circuit becomes low. The voltage swing at these nodes is suppressed, thus allowing low voltage operation. As the time constant at every node becomes low, high-speed and high-frequency operation also become possible while consuming relatively little power.

The drawback of current-mode circuits, however, is that precise current transfer is difficult. This is because no current feedback is possible and because the absolute value of the current is the concern. For example, the current transfer ratio error is large in a conventional current-mirror circuit due to device mismatches such as the threshold voltage (Vth) of transistors.

This situation poses challenges for attempts to achieve the high level of precision demanded by high-precision ADCs. Current-mode circuits have been avoided in high-speed and high-precision ADCs and a few published papers have advocated such designs [2], [3].

Reference 2 offered only a 6-bit solution. In [3], A 4 GS/s ADC with 7-bit ENOB was realized by using 32, 125 MS/s, current-mode 8-bit ADCs in parallel. The performance of current-mode 8-bit ADCs was satisfactory; however, it was obtained using a 3.3 V supply voltage. It is not clear whether the same performance could be realizable with a supply voltage of less than 2 V. This also does not match the scaling trend of the LSI process.

The purpose of this paper is, therefore, to develop a high-speed current-mode ADC with more than an 8-bit level of accuracy using a supply voltage of less than 2 V so that current-mode ADCs can be used in the era of scaled CMOS processes.

II. CANCELING THE CURRENT-TRANSFER-RATIO MISMATCH

The basic current-mode circuit is a current-mirror. A current-mirror circuit has poor current-transfer-ratio error due to device mismatches [4]. Figure 1 shows a current-mirror circuit which has obtained current exchanging capability. Assume that transistors M1 and M2 are identical, operate in the saturation region, and only a device parameter, that is, the threshold voltage, is different. In Figure 1, the threshold voltage of M1 is Vth while that of M2 is $V_{th} + \Delta V_{th}$. When switches sw1s and sw2s are on and off, respectively, iout becomes

$$i_{out} = i_{in} - \beta(V_{GS} - V_{th})\Delta V_{th} + \beta(\Delta V_{th})^2 / 2, \qquad (1)$$

where β is the transconductance parameter of the transistors and V_{GS} is the gate to the source voltage and is common to M1 and M2. We exchange the role of transistors by making sw1s off and sw2s on. Now, iin flows in M2 and iout flows in M1. Then iout becomes

$$i_{out} = i_{in} + \beta(V_{GS} - V_{th})\Delta V_{th} - \beta(\Delta V_{th})^2 / 2. \qquad (2)$$

If we add equations (1) and (2), then we have an error-free current relationship between iout and iin. In this paper, we propose to use the circuit shown in Figure 1 as a current-mirror circuit in a bit-block of a current-mode ADC and to switch sw1s and sw2s on and off alternatively in every clock period.
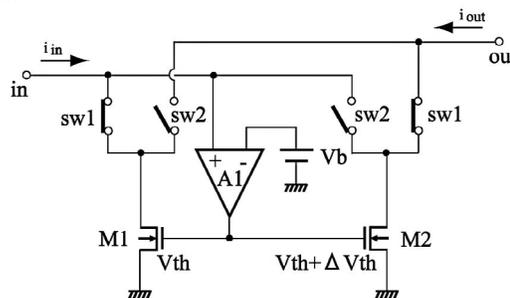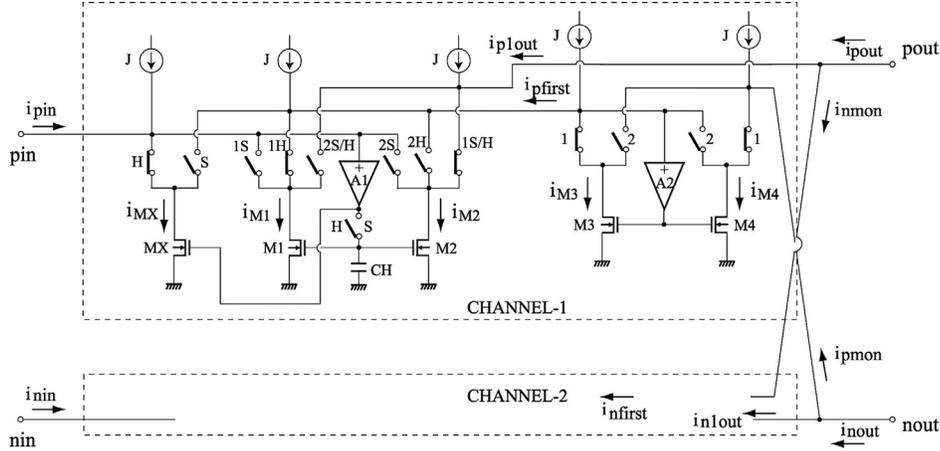

Fig. 1. An exchangeable current-mirror circuit.

Fig. 2. A bit-block circuit which doubles the input signal current with a current exchanging function.

III. A BIT-BLOCK CIRCUIT ARCHITECTURE

The bit-block that we have to realize has a 1.5-bit bit-block architecture. This requires a circuit that doubles the input current precisely within the error range in the n-bit ADC. This means that less than 0.1 % of the current ratio mismatch is required between the input and output current values of a bit-block when n equals 10.

In order to achieve this aim, our bit-block circuit could double the input signal current precisely by exchanging currents to cancel the current-transfer-ratio error of the current-mirror circuit. A circuit that realizes this operation is shown in Figure 2. This is a pseudo-differential circuit in which the positive input signal of the differential signal is applied to channel 1 and the negative input signal to channel 2. Channel 1 provides a copy of the positive input signal current and its inverted version, and channel 2 provides a copy of the negative input signal current and its inverted version. The copy of the positive input signal current in channel 1 and the inverted version of the negative input signal current in channel 2 are merged into one at the output of channel 1 to become the current ipout in Figure 2 with double the input current value. The same happens to inout shown in Figure 2.

The input signal current ipin flows into the terminal pin while inin flows into the terminal nin. As the signal is differential, ipin = − inin and inin in fact comes out of the terminal nin. Channel 1 contains two circuit blocks. One is a block which consists of transistors M1, M2, and Mx, an operational amplifier A1, a hold capacitor CH, 8 switches to exchange currents and 3 constant currents Js. We refer this as a "current exchanger." Another is a block which consists of transistors M3 and M4, an operational amplifier A2, 4 switches to exchange currents and 2 constant currents Js to invert the current value from positive to negative and vice versa. We refer this as a "current inverter."

The absolute current value at the output of the circuit shown in Figure 2 should be precise for the period when the input current is held constant. Moreover, we would like to

produce positive and negative errors in consecutive clock periods. The circuit shown in Figure 2 is in the hold mode of the first clock period. Switches in labels H, 1H, 1S/H, and 1 are on. The input signal current ipin flows into a transistor Mx so that the input terminal pin is not floating. In hold mode, the input signal current just before entering the hold mode is memorized in a transistor M1 by the role of CH and its mirror current flows into a transistor M2. As ipin flows into a transistor M1 when the circuit is in the sample mode in the first clock period, the current ipfirst in M1 in hold mode exactly equals the ipin in sample mode. The current ip1out in M2 becomes ipin $+ \Delta i11$, where $\Delta i11$ is the error caused by the current-transfer-ratio error from M1 to M2 in channel 1. The ipfirst is further inverted by the "current inverter" and, as a result, ipmon $= -$ ipin provided that the "current inverter" does not have current-transfer-ratio error. The same kind of operation occurs in channel 2, and infirst and in1out in channel 2 become equal to inin and inin $+ \Delta i12$, respectively. The $\Delta i12$ is the current-transfer-ratio error of the transistors in channel 2 that correspond to M2 and M1 of channel 1. The inmon becomes $-$inin as well. As a result, we obtain

$$\text{ipout} = \text{ipin} + \Delta i11 - \text{inin} = 2\text{ipin} + \Delta i11 \qquad (3)$$

$$\text{inout} = \text{inin} + \Delta i12 - \text{ipin} = 2\text{inin} + \Delta i12 , \qquad (4)$$

In the hold mode of the second clock period, switches H, 2S/H, 2H, and 2 become turn on. Just before entering the hold mode in the second clock period, the input signal current ipin flows in M2, and ipfirst becomes equal to ipin when the hold mode in the second clock period begins. The ipmon becomes $-$ipin as well. Then ip1out becomes ipin $-\Delta i11$, where $-\Delta i11$ is the transfer-current-ratio error from M2 to M1 and is the reciprocal value of $\Delta i11$ as indicated in equations (1) and (2). Similarly, infirst becomes inin; therefore, inmon becomes $-$inin while in1out is inin $-\Delta i12$, where $-\Delta i12$ is the current-transfer-ratio error from transistors in channel 2 that correspond to M2 and M1 of channel 1. We then obtain

$$ipout = ipin - \Delta i11 - inin = 2ipin - \Delta i11 \qquad (5)$$

$$inout = inin - \Delta i12 - ipin = 2inin - \Delta i12 , \qquad (6)$$

Equations (3) and (4) are currents at the outputs of a bit-block circuit shown in Figure 2 in the hold mode in the first clock period, and equations (5) and (6) are those in the hold mode in the second clock period. The addition of equations (3) and (5) produces the exact current value of 2ipin, and the addition of equations (4) and (6) produces the exact current value of 2inin. The above operation is performed by using two clock periods.

IV. THE DESIGNED CURRENT-MODE ADC

The designed current-mode pipelined ADC is shown in Figure 3. Each of the first three bit-blocks consists of the circuit shown in Figure 2, a sub-ADC and a sub-DAC. As the digitized reciprocal current mirror-ratio errors are obtained in the form of the digital data from a bit-block at consecutive clock periods, these two codes from the digital correction circuit shown in Figure 3 are added together to take the average by using a one-clock delay function (Z^{-1}) and an adder. A front-end current-mode S/H [4] samples the input signal for half the clock period and holds it for one-and-a-half of the clock period so that the ADC can digitize the same input signal level twice and produce positive and negative current-mirror ratio mismatch errors.

The sum of the output digital data from the adder appears in sequence with a clock; however, we need two data which are A-D converted when the front-end S/H are in hold mode. In order to collect the adequate data, one out of two is selected by using the MS-D-Latch which operates in half the clock frequency. This together with the addition forces the ADC reduce the sampling rate and signal frequency bandwidth by half.

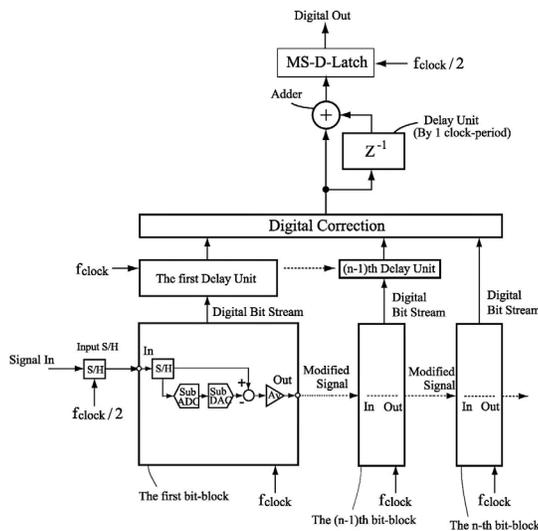It turns out that digital-assisted analog signal processing such as that involving exchanging currents in a bit-block by using switches and taking the sum, and therefore the average, of the A-D converted digital data in this case could enhance the analog performance that suffers from device mismatch errors. Since the current-mirror ratio errors of a current-mirror circuit is large, the above approach seems effective.
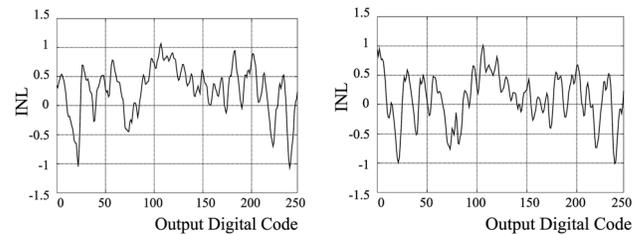
V. EVALUATION RESULTS

The current-mode ADC shown in Figure 3 is fabricated by using $0.25\,\mu m$ CMOS devices. The Z^{-1} function, an adder, and a MS-D-Latch seen in Figure 3 are external. A front-end S/H and 12 bit-blocks are installed on a chip. Although the chip has a 12-bit configuration, the achieved performance was at an 8-bit level and we thus decided to evaluate the test chip by taking only the upper 8 bits. The maximum usable clock frequency is 25 MHz and the power consumption is 60 mW from a power supply of 2 V. When the current exchange and averaging function are taken, the sampling speed and frequency bandwidth are reduced to 10 MHz and 5 MHz, respectively, even when the clock frequency is 20 MHz. In Figures 4 to 7, (b) shows the characteristics of this ADC. We refer this as the "double-sampling mode."
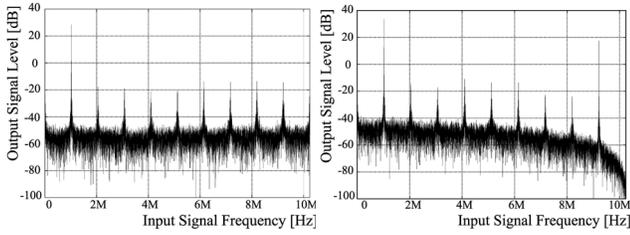
The test chip can also be configured to sample at a normal clock speed. In this case, the S/H operates with a 20 MHz clock and supplies a different held value to the ADC in each clock period. The function of taking the average of the output digital code is also stopped. However, the current exchange functions in the first three bit-blocks are active. We refer to this operation for reference purposes. In this case, errors are not canceled although they are produced in turn. We refer to this as the "single-sampling mode," and it is shown as (a) in Figures 4 to 7.
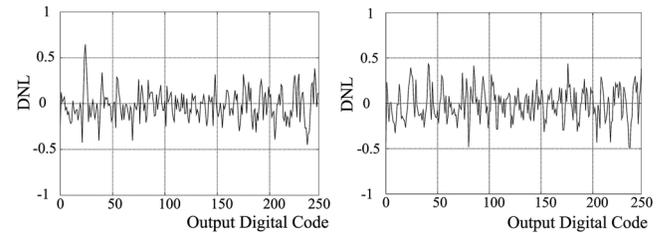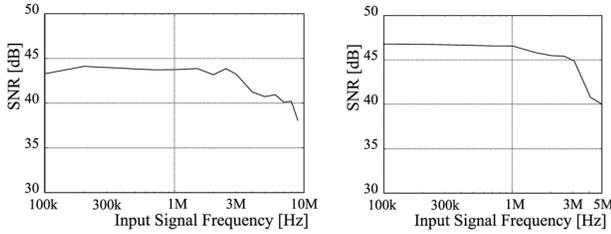

(a) Single-sampling mode (b) Double-sampling mode
Fig. 4. DNL errors (8-bit equivalent).

(a) Single-sampling mode (b) Double-sampling mode
Fig. 5. INL errors (8-bit level equivalent).

Fig. 3. A current-mode ADC which has bit-blocks with current exchange function , a front-end S/H, and averaging function of the output digital data.

(a) Single-sampling mode   (b) Double-sampling mode
Fig. 6. Frequency spectrum (FFT results of the ADC output).

(a) Single-sampling mode   (b) Double-sampling mode
Fig. 7. SNR frequency characteristics.

Figure 4 and Figure 5 show the measurement results of DNL and INL errors, respectively. The clock is 20 MHz and the input is the sinusoidal waveform at 10.1 KHz. The collected data points are approximately 200,000. The DNL error in Figure 4(b) is from +0.44 LSB to −0.49 LSB while that in Figure 4(a) is from +0.64 LSB to −0.45 LSB. An improvement is observed for the double-sampling mode over the single-sampling mode.

Figure 6 shows the frequency spectrum. The input signal frequency is 1 MHz and is at the full-scale level. The front-end S/H accepts a current signal which is converted from the full-scale 400 mV peak-to-peak voltage signal by using an on-chip 2 kΩ resistor. The full-scale level of this ADC becomes equal to ±100 μA of the input current. In case of the single-sampling mode, the fifth harmonic is the largest at −42 dB while in the double-sampling mode, the second harmonic is the largest at −48 dB together with the null at 10 MHz in frequency. Since the technique proposed in this paper corrects errors that come from the current-mirror ratio mismatch of a current-mirror circuit, the distortion should be the major characteristic that we have to focus on. A reduction of the distortion level can be clearly observed.

Figure 7 shows the SNR (signal-to-noise) characteristics. The proposed method does not affect the SNR; however, the quantization noise should be decreased by 3 dB because the frequency bandwidth is reduced by half (5 MHz) in the case of the double-sampling mode due to addition and averaging. Instead, the frequency bandwidth is 10 MHz in the case of the single-sampling mode. The SNR data in Figure 7(b) does not reach the quantization noise level of 49.7 dB and there must exist more noise components than the quantization noise.

Table 1 summarizes the performance of the ADC both in the single-sampling mode and the double-sampling mode.

DNL and INL errors and power consumption are calculated at an 8 bit level.

Table 1. Overall IC performance both in a single-sampling mode and a double-sampling mode.

	Single-sampling mode	Double-sampling mode	Units
Supply voltage	2	2	V
Max.clock frequency	25	25	MHz
DNL (8-bit , (20 MS/s)	+ 0.64 - 0.45	+ 0.44 - 0.49	LSB
INL (8-bit , (20 MS/s)	+ 1.1 - 1.1	+ 1.0 - 1.0	LSB
SNR (fin 1MHz F.S., 20 MS/s)	43.5	47	dB
SFDR (fin 1MHz F.S., 20 MS/s)	42	48	dB
Power consumption	60	60	mW
Process	CMOS 0.25	CMOS 0.25	um

VI. CONCLUSION

A current-mode ADC with current exchanging capability in a bit-block obtained through the use of a digital switching operation and with averaging calculation in the digital domain has been described. The performance of the proposed device was evaluated by the fabrication of a CMOS test chip using 0.25 μm transistors. The results show 8-bit level ADC realization with a clock speed of 25 MHz maximum from a 2 V supply voltage. Six dB and 0.2 LSB improvements in SFDR and DNL characteristics were observed. The effectiveness of the proposed method in a current-mode ADC has been verified.

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