A CMOS Current-mode DC-DC Converter with Input and Output Voltage-Independent Stability and Frequency Characteristics utilizing a Quadratic Slope Compensation Scheme

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***Abstract*— A CMOS Current-mode DC-DC converter using a quadratic slope compensation scheme is presented. The use of a quadratic slope instead of a conventional linear slope makes a damping factor and a frequency bandwidth of a current feedback loop independent of the converter's output voltage. Further designing the coefficient of the quadratic slope to be fully dependent of the input voltage, the damping factor and the frequency bandwidth become completely independent of both the input and output voltages. A test chip of a buck converter in a 5 MHz operation which uses a quadratic slope compensation scheme has been fabricated by using a 0.35 μm CMOS process. The evaluation results show that with a current capability of up to 500 mA the frequency characteristics of the total loop are constant when the input and output voltages change from 3.3 V to 2.5 V and from 2.5 V down to 0.5 V, respectively, and also that the recovery time is 50 μs with a peak voltage deviation of less than 50 mV for load current changes from 20 mA to 200 mA and vice versa.**

I. Introduction

Current-mode DC-DC converters become important as mobile equipment becomes increasingly popular. In such equipment, the powering on and off of LSIs as loads of the DC-DC converter repeatedly occurs. The settling time when the load current of the DC-DC converter suddenly changes becomes important because this determines the system speed. Under such conditions, a DC-DC converter with a current feedback loop is preferable to a converter with only a voltage feedback loop because it offers a large frequency bandwidth that far exceeds the resonant frequency of an external inductor and a capacitor those of which are commonly used to rectify the output pulse of the converter chip to the dc value.

Compared with a conventional voltage-mode DC-DC converter, the current-mode DC-DC converter has two feedback loops: one is a voltage feedback loop, and the other is a current feedback loop. The extension of the frequency bandwidth comes from the effect of the current feedback loop, which shortens the converter's settling time [1]. However, this current feedback loop needs a slope compensation to maintain its stability when the duty cycle of the output pulse exceeds 50%. A linear slope compensation scheme is commonly adopted, but loop frequency characteristics and stability criteria change depending on the converter's input and output voltages. The amount of slope compensation should be adjusted depending on usages of the converter.

We have proposed use of the quadratic slope compensation scheme to make loop frequency characteristics and the stability criteria constant and also to make the frequency bandwidth large so that the settling time becomes faster and constant, even when the input and output voltages of the DC-DC converter change [2]. In this paper, the effect of the quadratic slope compensation scheme is demonstrated by evaluation results from a test chip of a current-mode buck DC-DC converter by using a 0.35 μm CMOS process.

II. The current-mode DC-DC buck converter

Figure 1 shows a block diagram of the converter. It has two control loops: one is a voltage control loop; the other is a current control loop. The current detection circuit detects the inductor current and then converts it into voltage. The sum Vi of voltages from the current detection circuit and the slope compensation block is applied to a comparator and is

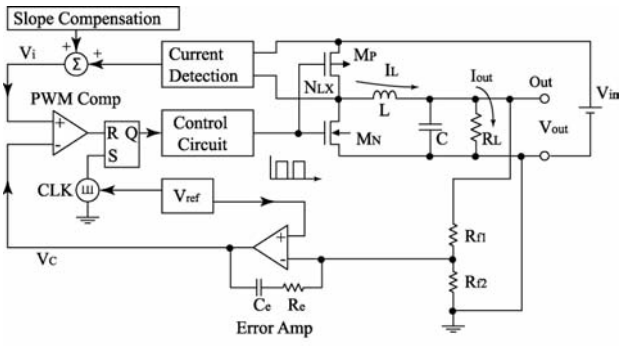

Fig. 1. Block diagram of the current-mode DC-DC buck converter.

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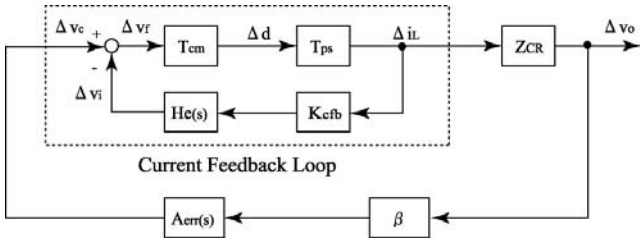
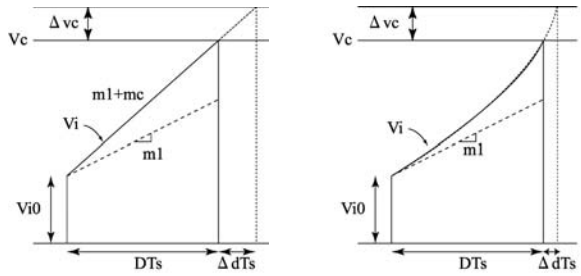


Fig. 2. Block representation of the current feedback loop.



(a) linear slope. (b) quadratic slope.

Fig. 3. Waveforms of linear and quadratic slope compensation.

compared with the voltage Vc from the error amplifier in the voltage control loop. The operation of this converter is as follows.

At the beginning of the clock period, a set pulse is applied to the S terminal of the SR-FF; this forces the Q output high. The output of the control circuit then becomes low, and M_p and M_n turn on and off, respectively. As a result, the inductor current I_L begins to increase in time. When V_i in Figure 1 which is the voltage proportional to the inductor current, exceeds V_c, the comparator output becomes high, and the Q output of the SR-FF becomes low. Then M_p and M_n change to off and on, respectively.

III. Frequency and Stability Analysis of the Current Feedback Loop

Figure 2 is a block representation of a DC-DC buck converter showing the current and the voltage feedback loops. T_{cm} is the transfer function from the feedback voltage to the duty cycle, T_{ps} is the transfer function from the duty cycle to the inductor current, $H_{e(s)}$ is the sampled-data transfer function, Z_{CR} is the impedance of C and the load resistor R_L in parallel, β is the voltage-dividing ratio between resistors R_{f1} and R_{f2} in Figure 1, and $A_{err}(s)$ is the small signal transfer function of the error amplifier. T_{ps} and $H_{e(s)}$ are given by

$$T_{ps} = \frac{\Delta i_L}{\Delta d} \cong \frac{V_{in}}{sL} \quad (1)$$

$$H_{e(s)} \cong 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{{\omega_n}^2} \quad (2)$$

where $\omega_n = \pi f_s$ and $Q_z = -2/\pi$ [3].

A. The Linear Slope Compensation

The current feedback loop, enclosed by the dashed line in Figure 2, is analyzed. In the case of the linear slope compensation, T_{cm} becomes

$$T_{cm} = \frac{\Delta d}{\Delta v_c} = \frac{f_s}{m_1 + m_c} \quad (3)$$

as shown in Figure 3, where m_c is the voltage slope of the slope compensation signal, and f_s is the converter's clock frequency. m_1 $\{= K_{cfb} \cdot (V_{in} - V_{out})/L\}$ is the slope of the inductor current change, which is converted into voltage in the current detection circuit. The closed-loop transfer function of the current feedback loop becomes

$$\frac{\Delta i_L}{\Delta v_c} = \frac{T_{cm} T_{ps}}{1 + K_{cfb} \cdot H_{e(s)} \cdot T_{cm} \cdot T_{ps}} \quad (4)$$

$$= \frac{1}{K_{cfb}} \cdot \frac{1}{1 + \frac{2s}{\omega_n}\zeta + \frac{s^2}{{\omega_n}^2}} \quad (5)$$

The damping factor ζ is

$$\zeta = \frac{\pi L}{2 V_{in} K_{cfb}} (m_1 + m_c) - \frac{\pi}{4} \quad (6)$$

The stability and the frequency bandwidth are deeply related to the ζ value in Eq. (6). In order to keep the stability of the current feedback loop, $\zeta \geq 1/2$ is necessary. When ζ becomes larger than one-half, the frequency bandwidth of the current feedback loop decreases. From Eq. (6), the m_c that satisfies the relation $\zeta \geq 1/2$ becomes

$$m_c \geq \frac{K_{cfb}}{L} \left\{ \left(\frac{1}{\pi} - \frac{1}{2} \right) V_{in} + V_{out} \right\} \quad (7)$$

The m_c is dependent on V_{in} and V_{out}. We need to set the m_c value each time depending on the various input and output voltages. Usually, we choose the maximum m_c that satisfies Equation (7) all the time for different V_{in}s and V_{out}s. As a result, the frequency bandwidth decreases. This becomes overcompensation when the input and output voltage of the DC-DC converter is low.

B. The Quadratic Slope Compensation

When we apply the quadratic slope compensation scheme, we need to examine two cases: a small signal condition and a large signal condition. In a steady state, the damping factor ζ should be larger than one-half. On the other hand, ζ should be larger than zero when a large amount of disturbance is introduced.

Figure 3(b) shows the waveform of V_i when the quadratic slope compensation is used. In a steady state,

$$V_c = m_1 D T_s + {m_c}' (D T_s)^2 + V_{i0} \quad (8)$$

where ${m_c}'$ is the coefficient for the quadratic slope compensation voltage, and V_{i0} is the voltage of V_i at time zero. When

V_c increases or V_i decreases by the amount Δv_c, we obtain

$$V_c + \Delta v_c = m_1 (D + \Delta d) T_s + m_c{}' \{(D + \Delta d) T_s\}^2 + V_{i0} \quad (9)$$

assuming that Δd is sufficiently small compared with D. In this case, T_{cm} is

$$T_{cm} = \frac{\Delta d}{\Delta v_c} = \frac{f_s}{m_1 + 2 m_c{}' D T_s} \quad (10)$$

Note that only the damping factor ζ becomes different from the case of the conventional linear slope compensation. Substituting Eq. (10) into Eq. (5), we obtain

$$\zeta = \frac{\pi L}{2 V_{in} K_{cfb}} \left(\frac{V_{in} - V_{out}}{L} K_{cfb} + 2 m_c{}' D T_s \right) - \frac{\pi}{4} \quad (11)$$

As mentioned before, ζ must be more than one-half. Then $m_c{}'$ becomes

$$m_c{}' \geq \frac{V_{in} f_s K_{cfb}}{2L} \left\{ 1 - \left(\frac{1}{2} - \frac{1}{\pi} \right) \frac{1}{D} \right\} \quad (12)$$

The lower limit of the $m_c{}'$ value is obtained by setting $D = 1$. From Eq. (12), we can find that the $m_c{}'$ value is not dependent on the output voltage but rather on the input voltage. Furthermore, in preparation for a large amount of disturbance, the effective slope value $m_{c(eff)}$ should be increased a little bit, and therefore, we choose the $m_c{}'$ value as

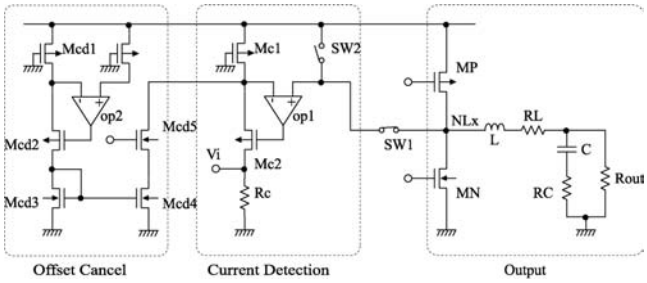
$$m_c{}' = \frac{V_{in} f_s K_{cfb}}{2L} \quad (13)$$

Substituting Equation (13) into Equation (11), the constant ζ value of $\pi/4$ is obtained. Thisw means that the frequency bandwidth of the current feedback loop does not change at any time if $\omega_n = \pi f_s$ is constant.

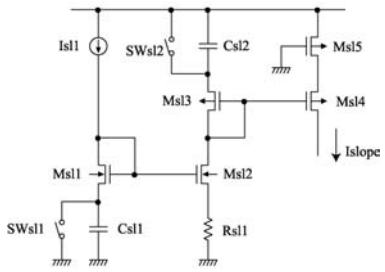
IV. The circuit implementation

In a proposed CMOS current-mode DC-DC converter, we need to have the constant current-to-voltage conversion gain K_{cfb} in the current detection circuit and the coefficient $m_c{}'$ of the quadratic current to be dependent on the input voltage. Circuits that realize these conditions are shown in Figure 4.

Figure 4(a) is the current detection circuit. It should detect the current that flows in an inductor L in the output block when a PMOS transistor MP turns on. When the circuit is in the current detection mode, SW1 turns on while SW2 turns off. By using an op-amp. op1 and the Mc2 in the current detection block, the drain-to-source voltages V_{ds}s of MP and Mc1 become equal. All the terminal voltage becomes equal in MP and Mc1 when MP turns on and the current flowing in Mc1 is proportional to the current flowing in MP. The current ratio is determined only by the size of these transistors and does not depend on the input voltage. The slope voltage Vi appears across the resistor Rc. Since the same current as in Mc1 flows through the resistor Rc, the constant conversion gain K_{cfb} is obtained. The offset cancel circuit in Figure 4(a) inhibits the extra current flow in the resistor Rc when SW1 turns off and SW2 turns on.



(a) the current detection circuit.



(b) The quadratic slope generation circuit.

Fig. 4. Circuits to obtain the constant K_{cfb} and the input voltage-dependent $m_c{}'$ value.

Figure 4(b) is the quadratic slope generation circuit. When MP turns on, the quadratic slope is generated. This is initiated by turning off switches SWs11 and SWs12. When Isl1 is the constant current, the voltage across the capacitor Cs11 increases as the time t increases, as a result, a current in the resistor Rsl1 increases in proportion to t. This current in the resistor Rsl1, again, produces a voltage across the capacitor Csl2 which is proportional to the time t. The resultant voltage across Csl2, therefore, becomes proportional to t^2. Assuming that the gate-to-source voltage of Ms14 and Ms15 does not change and that the on resistance of Ms15 is $1/\beta_{s15} (V_{in} - V_{ths15})$, the current I_{slope} becomes

$$I_{slope} = \frac{I_{s11} \beta_{s15} (V_{in} - V_{ths15})}{R_{s11} C_{s11} C_{s12}} t^2 \quad (14)$$

Equation 14 means that I_{slope}, the quadratic current, depends on the input voltage V_{in} of the converter.

V. Experimental results

A test chip that adopts the proposed quadratic slope compensation scheme was designed, fabricated and evaluated by using a 0.35 μm CMOS process. Because he process allows the maximum supply voltage to be only 3.3 V, the test chip suffered from this regulation. The output inductor L (2.2 μH), a capacitor C (10 μF), a load resistor R_L, feedback resistors R_{f1} and R_{f2}, and feedback elements of an error amplifier

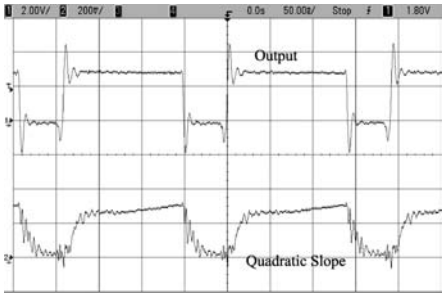


Fig. 5. Waveforms of the output signal and the quadratic slope.

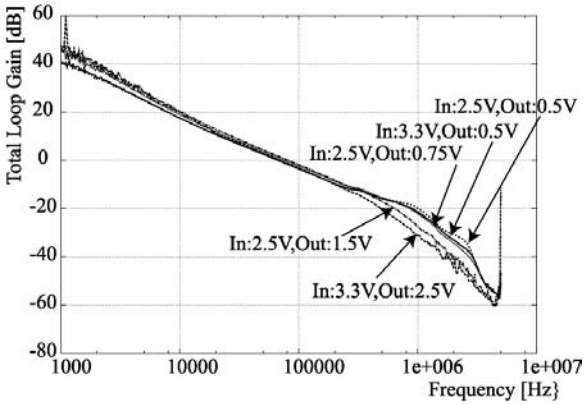


Fig. 6. Frequency characteristics of the combined total loop gain.

C_e (100 pF) and R_e (240 kΩ) in Figure 1 are all external components. The reason why C_e and R_e are external is that they accompany stray capacitors which change the frequency characteristics of the voltage loop in a DC-DC converter. The clock frequency is fixed to be 5 MHz.

Figure 5 shows waveforms at the Out terminal and a quadratic slope signal V_i shown in Figure 1 when V_{in}, V_{out} and I_{out} are 3.3 V, 2.5 V and 250 mA, respectively. The slope is definitely not linear. We added a circuit to monitor the waveform.

Figure 6 shows the open-loop frequency characteristics of the combined loop of the voltage and current loops in series. Those two loops cannot be separated. They are measured by injecting the signal from a 50 Ω resistor which is connected between the Out terminal and a feedback resistor R_{f1} and by observing the amount of signal which comes out at the Out terminal in Figure 1. There are five curves with different input and output voltages ranging from 3.3 V to 2.5 V and 2.5 V to 0.5 V, respectively. Up to 300 KHz of frequency and -10 dB of loop gain no difference for any can be seen. The loop gain increases when the output voltage of the DC-DC converter is close to its minimum value of 0.5 V at a frequency above 300 KHz. However, the duty ratio under these conditions is less than 50% and the slope compensation has no effect. The frequency characteristics are well behaved for output voltages of 1.5 V and 2.5 V with input voltages of 2.5 V and 3.3 V, respectively.

Figure 7 shows the transient response when the load current

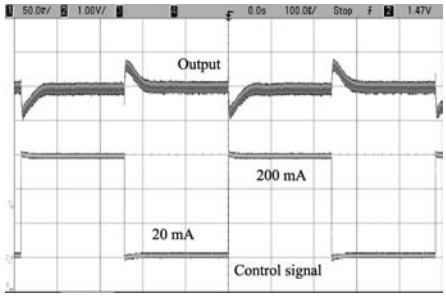


Fig. 7. The transient response for the load current change.

Table 1. Performance of a test chip

Input Voltage	3.3 V ∼ 2.5 V
Output Voltage	2.5 V ∼ 0.5 V
Max. Load Current	500 mA
Load Current Change (200 mA ∼ 20 mA)	50 μs less than 50 mV
Output Ripple	-48 dBm (2nd Harmonic)
Efficiency (In:3.3 V, Out:2.5 V)	85 % (Iout=100 mA)
Process	0.35 μm CMOS
Max. Voltage Tolerance	3.3 V

changes from 20 mA to 200 mA and vice versa. The upper curve is the voltage waveform at the Out terminal, and the lower curve is the control signal which changes the load current. When the control signal is high, the load current becomes 200 mA. A settling time of 50 μS with a voltage deviation of less than 50 mV has been observed.

Table 1 summarizes the performance of the test chip.

VI. Conclusion

A CMOS current-mode buck DC-DC converter has been realized by adopting a quadratic slope compensation scheme. The frequency characteristics become constant, and the settling time becomes short. A stable operation was realized for wide input and output voltages ranging from 3.3 V to 2.5 V and 2.5 V to 0.5 V, respectively, up to a load current of 500 mA. The effect of the quadratic slope compensation scheme is verified.

Acknowledgment

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References

[1] K.C. Wu, Pulse Width Modulated DC-DC Converters, CHAPMAN & HALL, 1997.

[2] H.Sakurai and Y.Sugimoto, "The Analysis and the Design of a Current-mode PWM Buck Converter by adopting the output-voltage independent Second-order Slope Compensation scheme," IEICE Trans. Fundamentals, vol.E88-A, no.2, pp.490-497, February 2005.

[3] R.D.Ridley, "A new, continuous-time model for current-mode control," IEEE Trans. Power Electron., vol.6, no.2, pp.270-280, April 1991.