A Synchronous, Step-down from 3.6V to 1.0V, 1MHz PWM CMOS DC/DC Converter

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Abstract

A new, synchronous, step-down from 3.6V to 1.0V, 1MHz PWM CMOS DC/DC converter IC with light-load mode control capability was developed. The power efficiency reached 80% at 80mA of load current, with a ripple of less than 20 mV. Only a 10μH and 47μF external inductor and capacitor, respectively, are needed.

1 Introduction

A lithium-ion battery whose voltage ranges from 3.6V to 3.0V is widely utilized in mobile information and communication equipment. On the other hand, it is LSIs that bring those equipments in commercial. LSIs' supply voltages decrease because LSIs are severely limited by device breakdown voltages and because they need to achieve low power dissipation. A large difference exists between the battery voltage and the LSI supply voltage. In order to fulfill this difference, a step-down DC/DC converter is used [1]. However, it is usually difficult to achieve high power efficiency for a step-down DC-DC converter with the battery voltage as an input and with an output voltage below 1V. Thus there exists an urgent need to improve the DC-DC converteter's power efficiency.

We have tried to realize a step-down DC/DC converter with an input voltage of 3.6V and with an output voltage below 1V together with a power efficiency of more than 80%. This paper describes the device's design and experimental results.

2 DC/DC converter architecture

Our purpose is to realize a new step-down DC/DC converter having the features described above. In order to realize these requirements, we adopted a fixed-frequency PWM-type converter structure as shown in Figure 1.

The frequency of the triangular waveform is 1MHz and a light-load mode control capability is included. The output circuit consists of PMOS (MP) and NMOS (MN) transistors which are connected in series between Vin and ground terminals. There is a feedback loop between Vout and the input of an error amplifier. The voltage difference between the Vout and Vref is amplified by the AC error amplifier. A comparator then compares the voltage between the output of the error amplifier and the output of a triangular waveform generator. The pulse width of the comparator output depends on the voltage at the FBin terminal, that is, Vout. The feedback for stabilizing the output voltage Vout is thus established. After that, this PWM signal is modified and applied to the gates of output

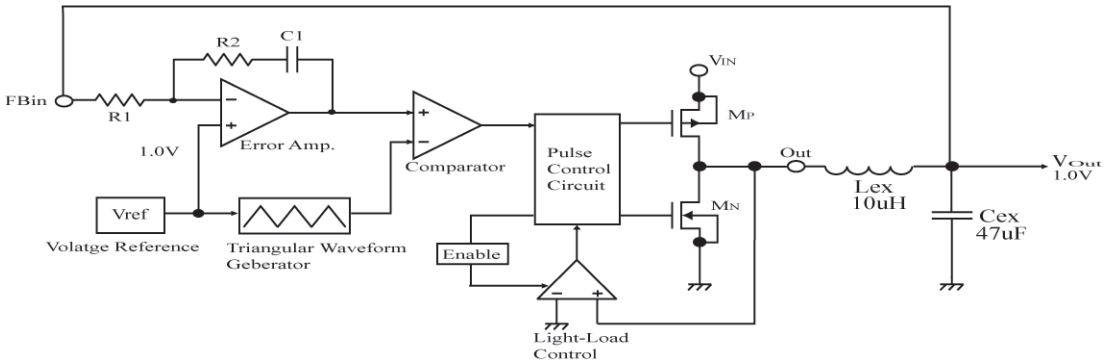

Fig. 1: Block diagram of the newly designed DC/DC Converter

transistors in order to drive the external energy-storage components such as an inductor and a capacitor.

For controlling the operation in the light-load mode, a comparator is prepared in order to detect if the current flow in an external inductor is reversed. When reversal of the current occurs, energy stored in Cex becomes released through an inductor and a transistor MN, and therefore power efficiency is degraded. The pulse control circuit forces the MN to off when this condition is detected.

3 1.0V operational capability

As the output voltage becomes 1.0V, a reference voltage of that value independent of the temperature change is needed.

Figure 2 shows the circuit of the 1.0V voltage reference. Transistors M1 and M2 differ in its threshold voltage (Vth), while the currents flowing in these transistors are identical. In an actual circuit, I1 and I2 are formed by a current-mirror circuit. The gate-to-source voltage of M2 (VgsM2) becomes,

$$VgsM2 = Vth2 - (\sqrt{\beta 1/\beta 2})Vth1 \qquad (1)$$

where β 1 and β 2, and Vth1 and Vth2 are the trans-conductance parameters and threshold voltages of M1 and M2, respectively. In the case $\beta 1 = \beta 2$, VgsM2 becomes Vth2-Vth1. As Vth difference does not change with temperature changes [2],[3], VgsM2 also becomes independent of temperature change. The threshold voltage varies from process to process, as does the voltage Vref. We introduced a fuse trimming technique for R2 to obtain the constant Vref.

In a PWM-type converter, the pulse width during a fixed time interval changes due to the feedback operation so that the output voltage becomes constant. In this DC/DC converter, the fixed time interval is chosen to approximately 1μs and is determined as the repetition time of a triangular waveform, which is generated by the circuit shown in Figure 3. As the fixed time interval shortens, external component values decrease and diminish in size. The triangular waveform appears across the CT. The voltage across it increases and decreases linearly between the fixed upper and lower voltage levels. To make the repetition time of a triangular waveform constant, the constant Vref is utilized to set the upper and lower voltage levels. In Figure 3, the upper level at V- terminal becomes Vref when S1 and S3 turn on, while lower level becomes Vref/2. The lower level is determined by the charge redistribution between Cr1 and Cr2 when S2 is turned on. Capacitor values Cr1 and Cr2 are chosen to be equal. The amplitude of the triangular waveform is sligtly larger than 0.5V.

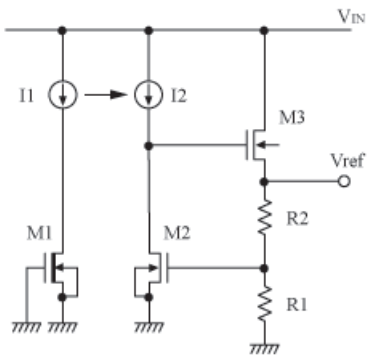

Fig. 2: 1.0V voltage reference

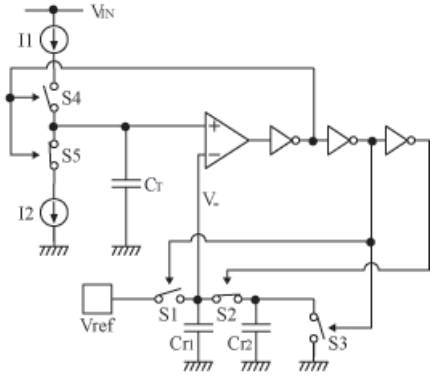

Fig. 3: Triangular waveform generator

4 High power efficiency realization

In the conventional step-down DC/DC converter, the power efficiency becomes extremely low when the input voltage is high and the output voltage is low. The converter uses a diode (commonly a shotkey diode) in place of the MN shown in Figure 1. This is very convenient because no direct current flows from Vin to ground. However, the voltage across the diode leads to a relatively large power consumption. In order to avoid this, a transistor MN is used as shown in Figure 4. In the figure, the MP turns on during the charge-up of an external inductor and MN turns on during the discharge interval. Since the on-resistance of a transistor is small, the power consumption also becomes small. However, there remains a danger for MN and MP to flow the direct current from the Vin to ground. This direct current, of course, should be avoided. A flip-flop with delays in it as shown in Figure 4 is introduced. A block denoted by a gate in Figure 4 is prepared in order to further improve the light-load mode condition. When the comparator output becomes high, the gate voltage of the MP immediately rises and that of the MN

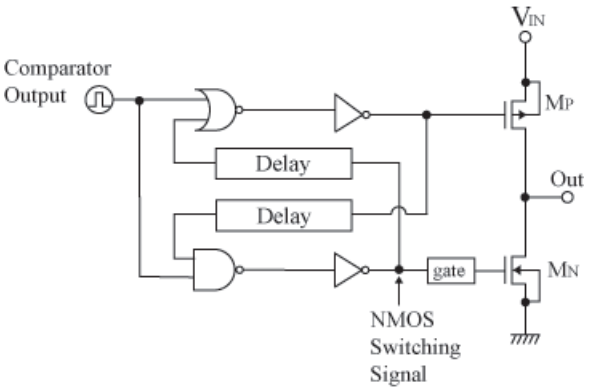

Fig. 4: Pulse control and output circuit

becomes high after a short delay time. When the comparator output becomes low, the gate voltage of the MN immediately falls and that of the MP decreases after a short delay time. This ensures the non-overlap operation of the control voltage for the MN and MP, thus eliminating the possibility of flowing direct current.

Figure 5 indicates how the reverse current flowing an inductor in light-load mode is inhibited. In a light-load mode, the energy stored in an inductor is released completely during the time interval when the MN in Figure 1 turns on. As the MN continues to turn on, the energy stored in a capacitor begins to be released. As a result, the reverse current flows in an inductor. Power is lost when this happens. In order to prevent this situation, the circuit shown in Figure 5(a) is introduced. The operation is further indicated in Figure 5(b). The reverse current can be detected by monitoring the waveform at the Out terminal as shown in Figure 1. When the reverse current begins to flow, the voltage at the Out terminal jumps from the negative value to the positive value. This is detected by the comparator at time B in Figure 5(a) and generates a reset signal for the S-R flip-flop. When a NMOS switching signal is applied to the circuit shown in Figure 5(a), the set signal for the S-R flip-flop is generated. Therefore, the driving signal for the MN gate finally becomes one such as that as shown in Figure 5(b). As a result, MN is activated only during the time interval between A and B when the energy is stored in an inductor.

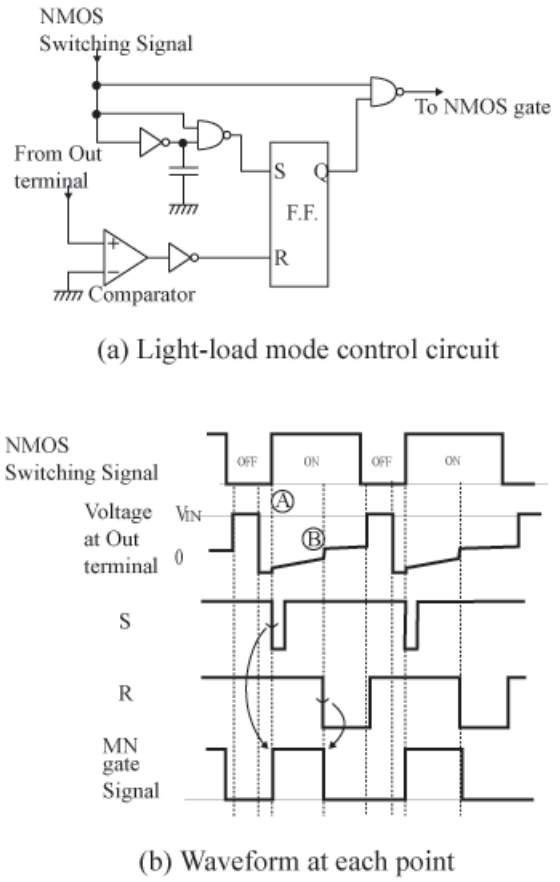

Fig. 5: Light-load mode control circuit

5 Evaluation results

The circuit is actually designed and fabricated by using MOS 2μm devices. Figure 6 shows load current vs. power efficiency characteristics. When Iload is 80mA, the power efficiency reached 80%. The on-resistance of the MP and MN was measured at 0.4 ohm and 0.3 ohm, respectively. If we assume that each MP and MN conducts half the duration of the fixed time interval, 2.2mW is consumed in these transistors. This is just 2.2% of the total power, allowing for further improvement in the future. The light-load mode operation is enabled by an external control terminal. Operation of the light-load mode control increases the power efficiency by about 20% when Iload is 5mA as can be seen in the figure. This verifies the effectiveness of the control below the load current of 20mA.

Figure 7 shows the output waveform which was measured across the capacitor Cex in Figure 1 when Iload is 100mA.The ripple was measured at less than 20mV.

Figure 8 shows the frequency spectrum of the Vout. The fundamental frequency of the fixed time interval was 1MHz and its magnitude was 5.1mV. The second harmonic was measured at 1.3mV.

Figure 9 verifies the light-load mode control operation when Iload is 10mA. The waveform is measured at the Out terminal shown in Figure 1. The MN in Figure 1 becomes off when the reverse current-flow in an inductor is detected, then free oscillation due to the external inductor and capacitor begins because they are left open in the loop which consists of an inductor, a capacitor, and the MN. The free oscillation waveform verifies that the MN is turned off during this interval. Table 1 summarizes the chip performance.

6 Conclusion

We were able to demonstrate the operation of a 3.6V input and 1.0V output CMOS DC/DC converter which realizes a power efficiency of more than 80%. We greatly thank the Ricoh corporation for fabricating the chip.

reference

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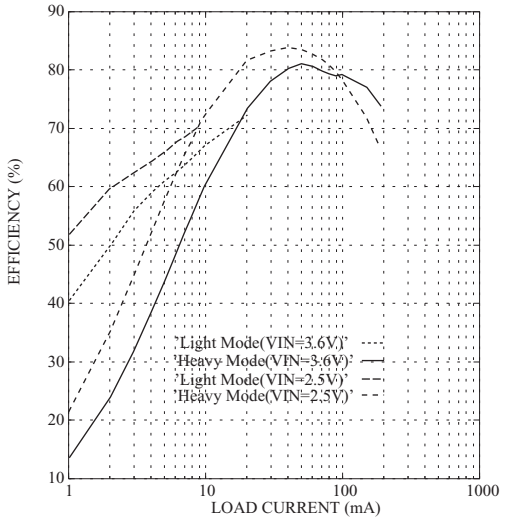

Fig. 6: Load current vs. power efficiency

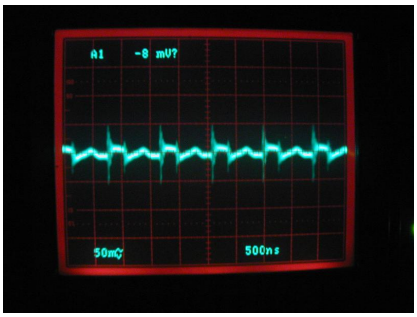

Fig. 7: Output waveforms

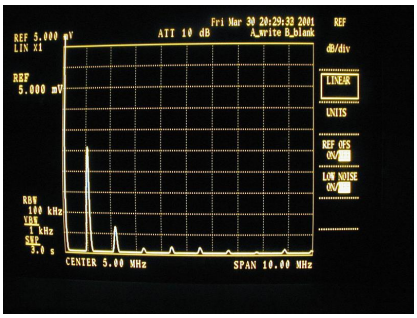

Fig. 8: Frequency spectrum of the output

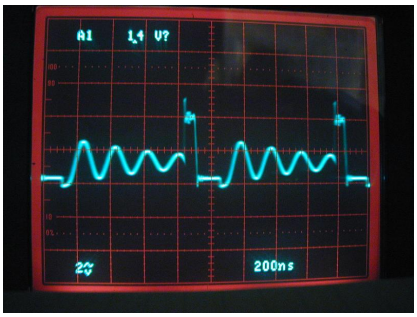

Fig. 9: Waveform at the out terminal in light-load mode

Tab. 1: Overall chip performance

Technology	2μm CMOS
Inductor(off-chip)	10μH
Capacitor(off-chip)	47μF
Switching Frequency	1MHz
Efficiency	80% @ I_{LOAD}=80mA 3.6V$\rightarrow$1.0V
Input Voltage	2$\sim$5V
output Voltage	1.0V
output ripple	$<$ 20mV