19-1

A 1V operational, 20Ms/s and 57dB of S/N, Current-mode CMOS Sample-and-hold IC

Yasuhiro Sugimoto

Department of Electrical, Electronic, and Communication Engineering, Chuo University
1-13-27, Kasuga, Bunkyo-ku, Tokyo 112-8551, Japan
Phone: +81-3-3817-1858 FAX: +81-3-3817-1847 E-mail: sugimoto@sugi.elect.chuo-u.ac.jp

Introduction

A 1V operational, 20Ms/s MOS sample-and-hold IC, which is applicable to video signal processing, has been developed. The signal-to-noise ratio (S/N) reached 57dB under the application of ±200uA of differential input signal current at an 1MHz frequency. The fabrication process was 0.35um CMOS with a threshold voltage of +0.35V for an NMOS and -0.35V for a PMOS.

Design Concepts for Realizing a 1V operational Video-rate Sample-and-hold IC

We have adopted four circuit design concepts in order to realize 1V operation, a clock speed of 20MHz, and a 10-bit S/N level. The first concept involves the use of a current-based circuit whose node voltage was fixed by using an operational amplifier [1]. At a supply voltage of 1V, it becomes very difficult to amplify the signal without distortion because the node voltage changes with the input signal. The second concept involves the use of a double sampling technique. This technique improves the frequency characteristics. Third, a gate voltage boosting technique was adopted to generate high gate voltages for analog switches. Finally, a full differential configuration was used. Even-order harmonics and common mode noise can be canceled out.

Circuit Design of a Sample-and-hold IC and its Evaluation Set-up

Figure 1 shows the whole circuit of the sample-and-hold IC. Three operational amplifiers, OP1, OP2, and OP3, are used for fixing constant node voltages (Vbias) at terminals A, B, and C without being affected by the signal current change. Although this leaves the problem how to design a low-voltage operational amplifier, 1V operation of the entire circuit becomes possible. For OP1, a higher gain is needed than for OP2 or OP3. This is because an external resistor is connected to A and complete fixing of this node is required in order to avoid distortion. Therefore, OP1 consists of an input differential amplifier and a folded-cascode output stage, while OP2 and OP3 consist of a single differential amplifier. A full-scale input signal current of ±200uA is chosen.

The current transfer and a sample-and-hold operation are performed by using a simple current-mirror circuit with an analog switch and a hold capacitor between transistor gates. MN1 and MN2, MN3 and MN4, and MP4 and MP5 form current-mirrors. SW1 and Ch1, and SW2 and Ch2 are sample switches and hold capacitors. The time when SW1 or SW2 becomes on is alternate, and a double sampling operation is performed. For each transistor in a current-mirror, a resistor, which consists of a transistor with its gate connected to Vcc or ground, is connected to its source. This reduces the influence of the Vth variation.

The circuit is full differential and has two equivalent circuit channels. At terminals OUT and OUT/, two signal currents from different channels are subtracted.

The on-resistance of an analog switch should be as low as possible. The newly designed gate-voltage boosting circuit is shown in Fig. 2. By connecting the bulk terminal of MP3 to the source terminal, the parasitic P-N junction diode between the source and bulk is eliminated and a high boosting voltage of 1.65V is obtained.

Figure 3 shows the evaluation circuit of the IC. Signals are supplied differentially through resistors Rin and Rin/. The output currents at OUT and OUT/ are converted to voltages and their difference are measured by using external operational amplifiers. Voltages at OUT and OUT/ are fixed to Vbias.

Experimental Results

We verified the 1V, 20 Ms/s operation and 57 dB of S/N of the sample-and-hold IC by fabricating a chip using the standard low-Vth CMOS 0.35μm process. Figure 4 shows a photograph of the test chip. The chip was fabricated as a part of the test chip. The Vths of the transistors were +0.35V for NMOS and -0.35V for PMOS.

Figure 5 shows the frequency spectrum of the output signal with a -10dB level of the full-scale input at a frequency of 1.3MHz with a 20MHz clock from a 1V power supply. The 2nd harmonic is observed at -52dB and the 3rd harmonic at -56dB below the fundamental. When the input level is increased to 0dB of the full-scale level, distortion of the input signal increases and the measurement becomes difficult. The noise level was observed at -67dB relative to the input signal level with an RBW of 100KHz. This equals 57 dB of S/N with a 10MHz signal bandwidth. The S/N value does not deteriorate even when the input signal is increased to the full-scale level.

Figure 6 shows the input and the output waveforms observed in the evaluation circuit in Figure 3.

Figure 7 shows the input signal frequency vs. the S/N characteristics which are measured with -10dB of full-scale level input at a clock rate of 20Msps from a 1V power supply. S/N does not significantly degrade up to the Nyquist frequency. This verifies the effect of double sampling.

Although the chip consumes 3mW of power in total, a full circuit configuration including differential structure, double sampling structure, and sufficient current values are adopted this time in order to obtain reliability and the characteristics.

Conclusions

We used 0.35μm CMOS devices to confirm the feasibility of a 1V operational sample-and-hold IC with a clock frequency of 20MHz and a S/N ratio of 57dB. The author would like to thank the NPC corporation for fabricating this chip.

References

[1] Y.Sugimoto, "A 1.5 V, 30 Msps, 9- to 10-bit equivalent Current-mode CMOS Sample-and-hold Circuit ; Proceedings of the 25th European Solid-State Circuits Conference, pp.378-381, September 1999.

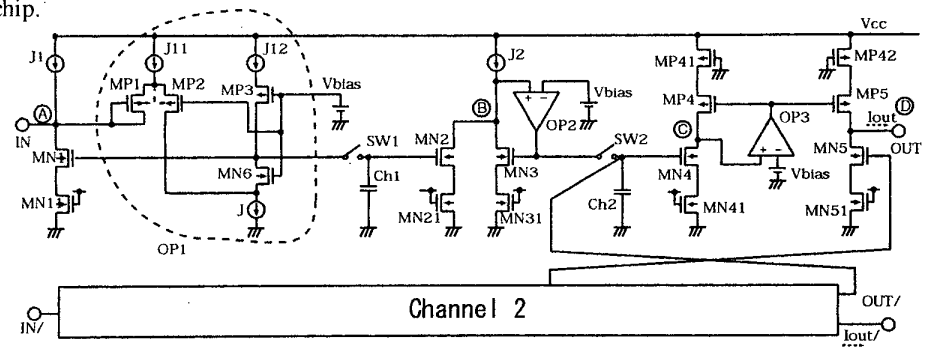

Fig. 1 Circuits of the fabricated sample-and-hold IC

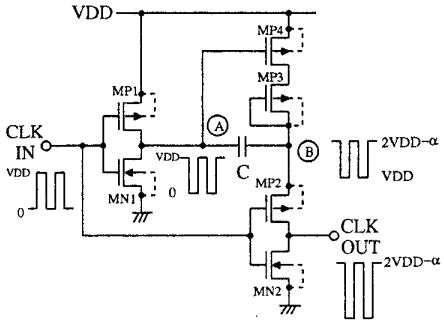

Fig. 2 Gate voltage boosting circuit

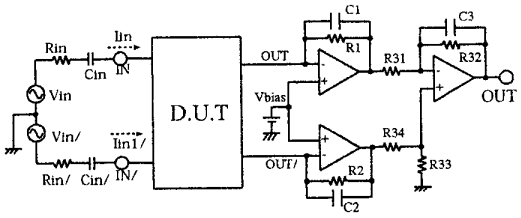

Fig. 3 Experimental set-up of the IC

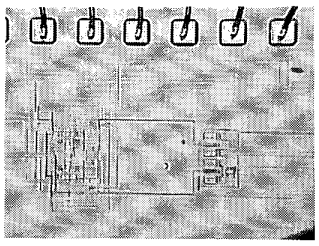

Fig. 4 Chip microphotograph

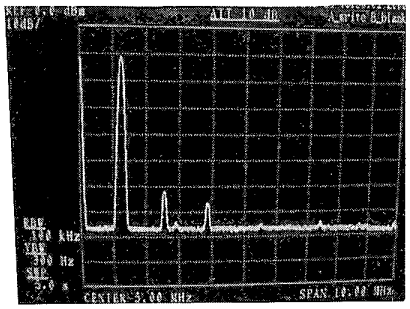

Fig. 5 Frequency spectrum of the output waveform (Input: -10dB of full-scale, fin=1.3MHz, fclk=20MHz, Vcc=1V, RBW=100KHz, VBW=300Hz)

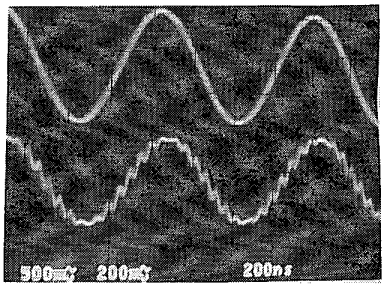

Fig. 6 Input and output waveforms (Upper: Input, fin=1.3MHz, 200 mV/div, Lower: Output, 500mv/div, fclk=20MHz)

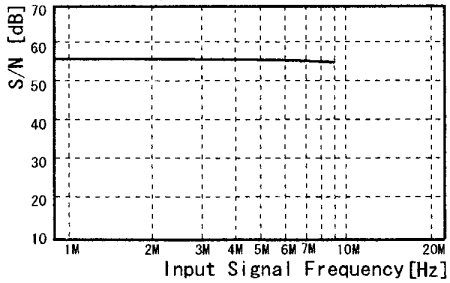

Fig. 7 Input signal frequency vs. S/N characteristics (Vcc=1V, fclk=20MHz, -10dB input of full-scale)