EFFECT OF A GROUND SHIELD OF A SILICON ON-CHIP SPIRAL INDUCTOR

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This paper proposes a new layout for a silicon on-chip spiral inductor and analyzes the effectiveness of a ground shield that is considered to enhance the quality factor of a spiral inductor on a silicon chip. The effective series resistance becomes low when a ground shield is placed under a spiral inductor. Furthermore, a spiral inductor with a surrounding ground shield (SGS) does not significantly improve the quality factor, but a spiral inductor with a patterned ground shield (PGS) may.

1 Introduction

Techniques for reducing the ohmic loss in a silicon substrate have been investigated by increasing the resistivity of the substrate[1]. However, this technique is not applicable to conventional LSI's. Another technique in which a ground shield is inserted between an on-chip spiral inductor and a silicon substrate has also been reported[2]. A silicon on-chip spiral inductor with a ground shield is said to realize high Q (quality factor) without being affected by the conductive silicon substrate. However, the reason or mechanism for improvement has not been clarified yet. It seems that the Q largely depends on the structure of the ground shield. In this paper, we attempt to determine the effect of a ground shield and to find an appropriate structure for a silicon on-chip spiral inductor.

2 Structures of examined spiral inductors

Figures 1 and 2 show layouts of on-chip spiral inductors with a different type of a ground shield.

![Figure 1: Surrounding Ground Shield (SGS)](image1)

![Figure 2: Patterned Ground Shield (PGS)](image2)

The structure of Fig. 1 was reported in reference [2], and a structure similar to that of Fig. 2, in reference [3]. The spiral inductor in reference [3] has a ground shield with its fingers...
extended to the center of the layout. Instead, we proposed the structure in Fig. 2 because we found that fingers inside a spiral inductor did not significantly affect the Q of the inductor. The ground shields consist of the first metal, and spiral inductors consist of the fourth metal assuming the standard 0.35μm MOS LSI process. The thicknesses of the fourth metal and the first metal are 0.92μm and 0.65μm, respectively. The thicknesses of the oxide between the first metal and the fourth metal, and between the silicon substrate and the first metal are 3.55μm and 1.1μm, respectively. The resistivity of the silicon substrate is 10Ω · cm. Each inductor has 10μm line width and 5μm line spacing. The ground fingers in Fig. 2 have 10μm line width and 10μm line spacing.

3 Equivalent circuit of a spiral inductor with a ground shield

The equivalent circuit of a silicon on-chip spiral inductor with a ground shield is shown in Fig. 3(a). $C_{ox1}$ is the oxide capacitance between a spiral inductor and the silicon substrate, and $R_{si}$ and $C_{si}$ are the shunt resistance and the shunt capacitance of a silicon substrate. $C_{ox2}$ is the capacitance between an inductor metal and the ground shield, and $C_s$ is the capacitance between inductor metals. $R$ and $L$ are the series resistance and inductance of a spiral inductor. This equivalent circuit in Fig. 3(a) is simplified in Fig. 3(b). Here, the effective shunt resistance $R_p$ and the effective shunt capacitance $C_p$ become

$$R_p = \frac{1}{\omega^2 C_{ox1}^2 R_{si} + R_{si}^2 + 2 \frac{R_{si} C_{si}}{C_{ox1}} + \frac{R_{si} C_{si}^2}{C_{ox1}^2}}, \quad (1)$$

$$C_p = C_{ox2} + C_{ox1} \frac{1 + \omega^2 R_{si}^2 C_{si}(C_{ox1} + C_{si})}{1 + \omega^2 R_{si}^2 (C_{ox1} + C_{si})^2}. \quad (2)$$

and the quality factor is calculated as [3]

$$Q = \frac{\omega L_s}{R_{si}} \frac{R_p}{R_p + R_{si} \left[ 1 + \left( \frac{\omega L_s}{R_{si}} \right)^2 \right]} \left[ 1 - \frac{R_{si}^2 C_p}{L_s} - \omega^2 L_s C_p \right]$$

$$= \text{unloaded } Q \times \text{substrate loss factor } \times \text{self-resonance factor} \quad (3)$$

The ground shield is known to decrease $C_{ox1}$ but increase $C_{ox2}$. This means that $R_p$ and $C_p$ increase in equations (1) and (2). It is not clear whether the Q is increased or decreased by this change in the equation (3).

4 Simulation results

In order to clarify the point described above, we conducted an electromagnetic field simulation using the HFSS simulation tool. Figure 4 shows the result. Here, NORMAL stands for a spiral
inductor without a ground shield. The SGS is shown in Fig. 1, and PGS, in Fig. 2. The Q of the PGS is lower than that of the NORMAL configuration in the low-frequency region, but higher in the high-frequency region. In contrast, the Q of the SGS is lower than that of the NORMAL configuration for all frequencies up to 5GHz.

In order to investigate the reason for this, we extracted the series component and the shunt component by the method shown in Fig. 5 using simulated S parameters.

Figure 4: Frequency characteristics of the quality factor

Figure 5: Extraction method for series and shunt components

Figure 6: Effective series resistance \( R_s \)

Figure 7: Capacitance changes of metal-to-metal capacitance \( C_s \) and metal-to-ground capacitance \( C_p \)

One thing that we notice from the result of this extraction is the change of \( R_s \) in frequency as shown in Fig. 6. The \( R_s \) of SGS is higher than that of the NORMAL configuration, but the \( R_s \) of PGS is lower than that of the NORMAL configuration at high frequency. It is very important to decrease \( R_s \) to improve Q as is apparent in the unloaded Q factor in equation (3). \( R_s \) is expected to increase when a conductor is placed close to the spiral inductor due to the effect of the eddy current. The reason the \( R_s \) of SGS increases in frequency can be explained as the influence of this eddy current. However, this does not explain the fact that \( R_s \) of PGS does not increase much in the high-frequency region. We thought that this comes from the decrease
of $C_s$, part of which is converted to part of $C_{ox2}$. In order to verify this, we calculated the values of the coupling capacitor $C_s$ and the line-to-ground capacitor $C_p$ of the ideal coupled parallel strip line, which correspond to $C_s$ and $C_{ox2}$ in Fig. 3(a), respectively. Figure 7 shows the result of this calculation. The horizontal axis is the distance ($h$) between lines and the ground plane. The line width ($W$) and spacing ($S$) were set to 10$\mu$m and 5$\mu$m, respectively. From Fig. 7, we can find that $C_s$ becomes smaller while $C_p$ becomes larger as the ground plane is placed closer to the lines. The calculation was performed using the following formula[4].

$$C_{os} = 4\epsilon_0 \frac{K(k_0)}{K(k'_0)}, \quad k_0 = \tanh \left( \frac{\pi W}{4} \frac{1}{h} \right) \coth \left[ \frac{\pi}{4} \left( \frac{W + S}{h} \right) \right]$$

$$C_{es} = 4\epsilon_0 \frac{K(k_e)}{K(k'_e)}, \quad k_e = \tanh \left( \frac{\pi W}{4} \frac{1}{h} \right) \tanh \left[ \frac{\pi}{4} \left( \frac{W + S}{h} \right) \right]$$

$$C_s = \frac{1}{2} (C_{os} - C_{es}), \quad C_p = \frac{1}{2} C_{es}.$$  

where $K(k)$ are complete elliptic integrals of the first kind with parameter $k$ and $\kappa' = \sqrt{1 - k^2}$. This fact implies that part of $C_s$ is converted to part of $C_p$ when the ground plane is placed close under the lines. The result of the analysis can easily be applied to explaining the characteristic in Fig. 4 and Fig. 6. For a spiral inductor in Fig. 2 (that is PGS), coupling capacitors between lines become small and line-to-ground capacitors become large. Therefore, the effective series resistance $R_s$ in Fig. 5 does not change much as the signal frequency increases. This is why the Q of PGS stays high in the high-frequency region. In contrast, line-to-ground capacitance increases, however this may not cause the decrease of self-resonant frequency of a spiral inductor because the effective inductance value $L_s$ changes.

5 Conclusions

We proposed a new layout for a silicon on-chip spiral inductor with a patterned ground shield. We tried to clarify how adopting a patterned ground shield produced high Q. As a result, we found that the coupling capacitor between lines in a spiral inductor decreases when a patterned ground shield is placed close under an inductor, and this reduces the effective series resistance, thereby increasing the Q of an inductor in the high-frequency region. We also found that line-to-ground capacitance increases.

References