A 1.5 V, 30 Msps, 9- to 10-bit equivalent Current-mode CMOS Sample-and-hold Circuit

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Abstract

A new video-speed, current-mode, CMOS, sample-and-hold circuit has been developed. It operates with a supply voltage as low as 1.5 V and a signal-to-noise ratio (S/N) of 57 dB and 54 dB at clock frequencies of 20 MHz and 30 MHz. It consists of current mirror circuits with an analog switch and a capacitor placed in differential form to achieve high accuracy without being affected by the switch feed-through error. Voltages at the input and the output terminals of the current mirror circuit are kept constant to obtain precise current matching. The circuit was fabricated using 0.6 μm MOS devices with normal threshold voltages (Vth) of +0 7 V (NMOS) and -0.7 V (PMOS).

1. Introduction

Today, LSI supply voltages are decreasing because LSIs are severely limited by device breakdown voltages and because they need to achieve low power dissipation. However, it is usually difficult to lower the voltage of analog circuits while preserving high-precision and high-speed characteristics. When the voltage range available for the signal is reduced, the signal-to-noise ratio and distortion deteriorate. The influence of reducing the supply voltage is therefore severe. Our approach to solve this problem is to use signal current instead of signal voltage as a carrier of information [1]. Low-power, low-voltage operation is possible because the voltage change in each node is suppressed. Furthermore, high-speed operation is possible because the impedance of each node becomes low. Until now, however, there has been no practical demonstration of the low-voltage, high-speed operation capabilities, except for low Q filters [2]. It is difficult to match input and output currents well, and this limits the overall performance of an analog circuit. This paper presents the design and evaluation results of a MOS sample-and-hold circuit that realizes 1.5 V operation, 30 MHz sampling and 9- to 10-bit level accuracy.

2. High-precesion current mirror circuit

Figure 1 shows the conventional MOS current mirror circuit which is configured as a low-voltage sample-and-hold circuit. M1 and M2 form a simple current mirror when SW1 is on, and input signal current is mirrored to the output. When SW1 turns off, the gate-to-source voltage of M2 at that time is memorized in Ch1. This voltage across the capacitor remains constant, so Iout becomes constant, accomplishing the input current hold operation. To convert the input voltage to the current, external resistor Rin is used. The voltage at terminal IN, however, changes nonlinearly as the input signal level changes as shown in the figure, introducing a signal-dependent current conversion error. The drain-to-source voltage of M1 also changes as input signal changes, resulting in a change of the current mirror ratio. The output voltage (Vout) is fixed in this case.

To resolve this issue, we should insert a positive amplifier between terminal IN and the gate of transistor M1. This is shown in Fig. 2. PMOS transistor M3 with its bulk terminal connected to Vcc and a current source Ib1 form the positive amplifier. In the figure, current (J+Iin) flows in n-channel transistor M1, while VNIN at terminal NIN is fixed by the gate-to-source voltage of p-channel transistor M3. The current through transistor M3 is the constant current Ib1; therefore, its gate-to-source voltage remains constant. The input voltage change Δ VNIN becomes

$$\Delta VNIN = (gds3/gm1gm3)Iin \quad (1)$$

where gm1 is the transconductance of transistor M1, and

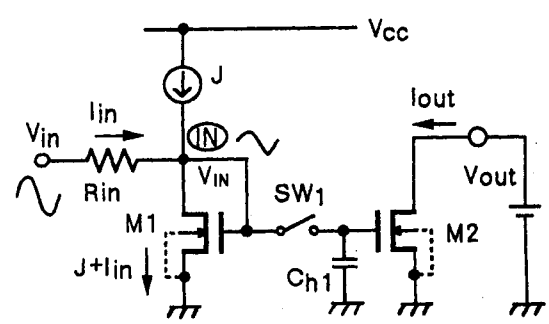

Figure 1. Conventional low-voltage sample-and-hold circuit

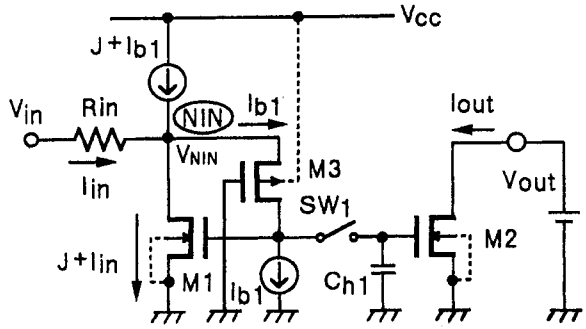

Figure 2. High-precision low-voltage sample-and-hold circuit

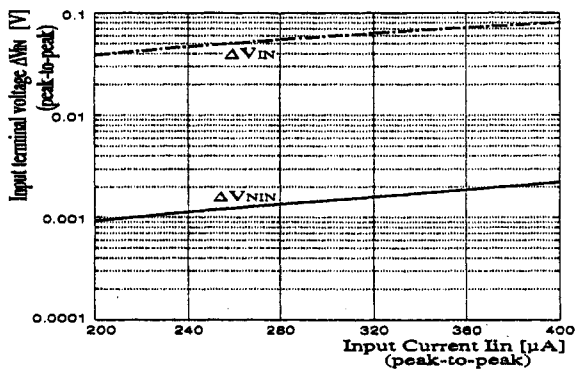

Figure 3. Voltage change at input terminals

gm3 and gds3 are the transconductance and output conductance of transistor M3. Equation 1 indicates that Δ VNIN becomes much smaller than in the conventional current mirror circuit due to the ratio gds3/gm3. This situation was SPICE-simulated as shown in Fig. 3. Δ VNIN shows the peak-to-peak voltage variation at terminal NIN in Fig. 2, while Δ VIN is that at terminal IN in Fig. 1. Excellent current matching is obtained for M1 and M2 in Fig. 2 because voltages of both the input and output terminals become constant. The input current change can be reproduced by using the voltage change at the gate of M1. The voltage VNIN at terminal NIN and drain-to-source voltage Vds3 of M3 become

$$VNIN = |Vthp| + \sqrt{2Ib1/\beta p}$$

$$Vds3 = VNIN - Vthn - \sqrt{2J/\beta n} \quad (2)$$

provided that J>Iin. Vthp and βp are the threshold voltage and the transconductance parameter of M3, and Vthn and βn are the those for M1. For M3 to operate in the saturation region, the conditions below are required.

$$|Vthp| > Vthn + \sqrt{2J/\beta n} \quad (3)$$

In this design, M3's bulk terminal is connected to Vcc, and M3's source terminal is connected to terminal NIN. This gives rise to the bulk effect, and Vthp becomes large. Therefore, the condition required in equation 3 is satisfied.

The minimum supply voltage of the circuit in Fig. 2 becomes VNIN plus the voltage necessary to maintain a current source J+Ib1. With Vthp of -1V, the minimum supply voltage is estimated to be roughly 1.5V, considering the bulk effect of M3.

3. Sample-and-hold circuit

The current-mode CMOS sample-and-hold circuit shown in Fig. 4 was designed. An input signal current of $\pm 200\mu$A is applied to terminal A through external resistor Rin. The circuit in Fig. 2 greatly suffers from clock feed-through error from analog switches. Differential placement of sample switches and cancellation of the clock feed-through are necessary [3]. In order to achieve high-precision current mirror operation, the drain voltages of transistors M2 and M12 are also kept constant by using the replica PMOS version of the circuit in Fig. 2. Voltages at both terminals A and C in Fig. 4 are constant, and the currents in M1 and M2 become independent of the input signal change. Voltages at out and out/ terminals are also kept constant because these terminals are assumed to be connected to the virtual ground of external operational amplifiers in the evaluation and to the same kind of constant voltage input terminals when this sample-and-hold circuit is used in combination with a current-mode A/D converter. Therefore, the currents flowing in M2, M4 and M5 are set equal. When clock feed-through error is generated in SW1, the voltage across Ch1 changes. Suppose that the current change -ΔI occurs in M2 due to the voltage change at Ch1. The currents flowing through M17, M4, and M5 then also change by -ΔI each. Because the same amount of clock feed through is expected to be injected from SW2 to Ch2, the same amount of current change as in M2 (-ΔI) is considered to be generated in M12, M7, M14 and M15. The current change caused by the switches' clock feed through in M5 is -ΔI, and that in M7 is also -ΔI. These two current changes cancel each other, and clock feed through will not influence the output current Iout. The same kind of clock feed-through cancellation occurs at terminal out/.

4. Experimental results

The circuit in Fig. 4 was fabricated using CMOS 0.6 μm devices. NMOS transistors have a Vth of +0.7 V, and PMOS transistors, -0.7 V.

Figure 5 shows input and output waveforms in the sample-and-hold mode with a 1.5 V supply and a 20 MHz clock. The upper waveform is the 1 MHz input with a full scale level ($\pm$1.02 V for a 5.1 K Ω resistor), and the lower waveform is the output. As the outputs of

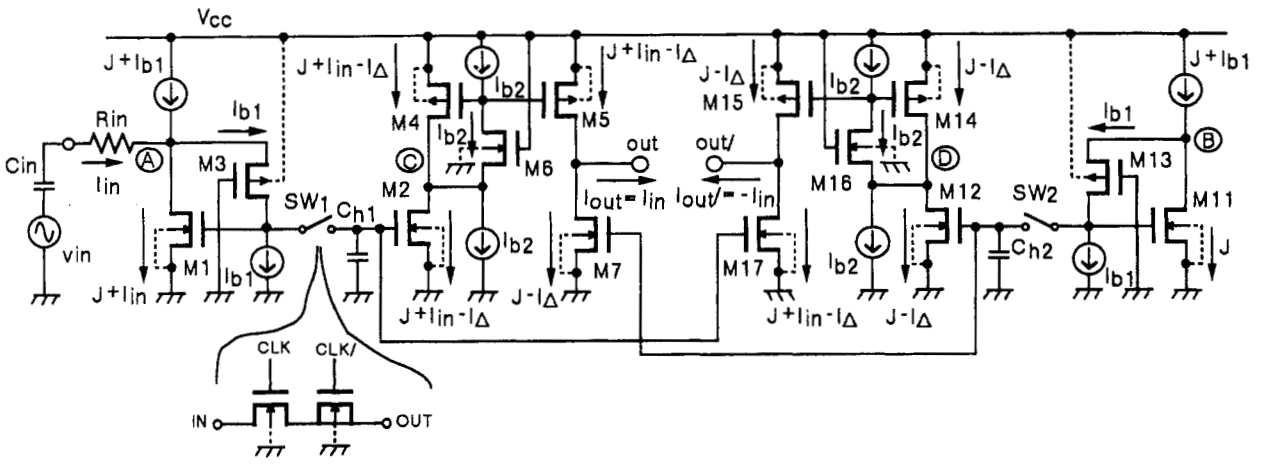

Figure 4. Low-voltage, high-performance sample-and-hold circuit

the chip are currents, they were converted to voltage by using external operational amplifiers on an evaluation board.

Figure 6 presents the results of a beat frequency test in which harmonics of the 9.9 MHz input signal (upper trace) are mixed with a 20 MHz clock and produce a beat frequency (lower trace). This test checks to what extent the circuit can track input amplitude changes.

Figure 7 illustrates the frequency spectrum of the output waveform with a 30 MHz clock. The input signal was full-scale with a frequency of 1 MHz. RBW was 100 KHz; VBW, 1 KHz; and frequency span, 15 MHz. The observed noise level was -85 dBm, while the fundamental, second, and third harmonics were -10 dBm, -58 dBm and -59 dBm, respectively.

Figure 8 shows the signal-to-noise ratio with changing input signal frequency in the sample-and-hold mode. The bold line shows the S/N value when the clock frequency was 30 MHz; the chained line shows the S/N with a 20 MHz clock. The S/N at low frequency reached 54 dB and 57 dB for clocks 30 MHz and 20 MHz. The S/N was not significantly degraded even for a 15MHz input signal. We can conclude that the S/N was 9-bit level for a 30 MHz clock and 10-bit level for a 20 MHz clock.

Figure 9 shows a photograph of the chip, and Table 1 summarizes the chip's overall performance. Power dissipation was 2.3mW.

5. Conclusion

We were able to demonstrate 1.5V operation of a 30Msps CMOS current-mode sample-and-hold circuit. This was achieved using transistors with normal Vth values.

6. Acknowledgement

The author would like to thank Ricoh Corporation, Tokyo for fabricating the chip.

7. References

[1] C.Toumazou, J.B.Hughes & N.C.Battersby, " SWITCHED-CURRENTS an analogue technique for digital technology " , IEE circuits and systems series 5, Peter Peregrinus Ltd., 1993.

[2] Lu P.H., Wu C.Y. and Tsai M.K., " Design Techniques for Tunable Transconductance-C VHF Bandpass Filters ", IEEE J.Solid State Circuits, Vol.29, No.9, pp.1108-1116, September 1994.

[3] Sugimoto Y., Tokito S., Kakitani H. and Seta E., " A current-mode bit-block circuit applicable to low-voltage, low-power pipeline video-speed A/D converters ", IEICE Trans. Fundamentals, vol.E79-A, no.2, pp.199-209, February 1996.

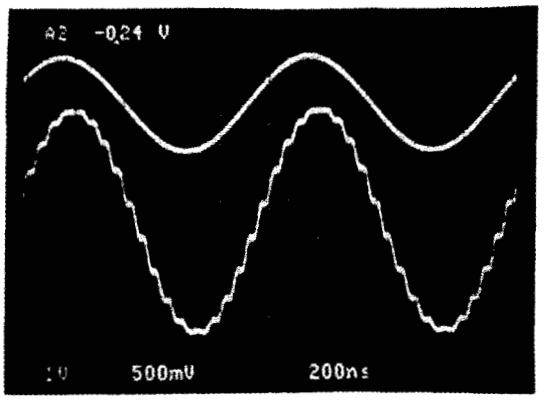

Figure 5. Input and output waveforms (fin=1 MHz, 0 dB full scale input, Vcc=1.5 V, clock=20 MHz)

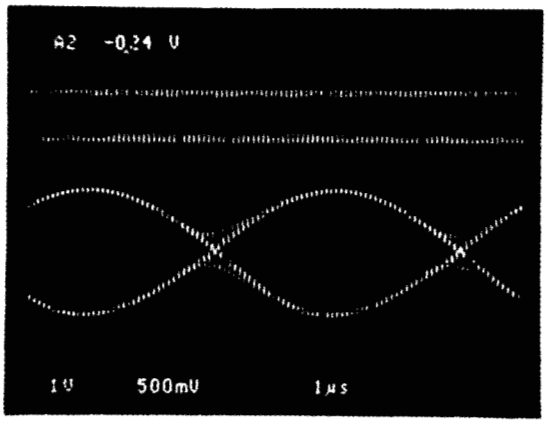

Fig. 6 Result of the beat frequency test
(upper, In; lower, out; fin=9.9 MHz, 0dB of full scale; Vcc=1.5 V; clock=20 MHz)

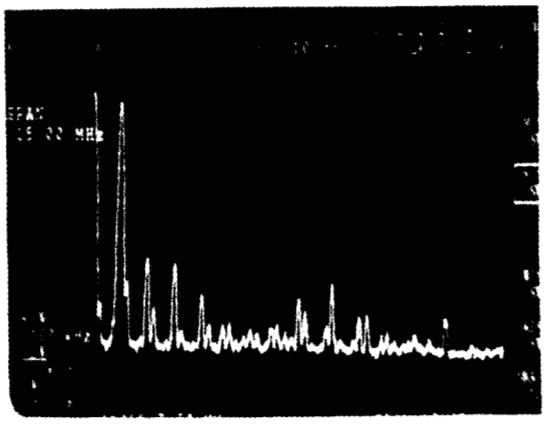

Figure 7. Spectrum of the output signal
(fin=1 MHz, 0 dB full scale input, Vcc=1.5 V, clock=30 MHz, RBW=100 KHz, VBW=1 KHz, span=15 MHz)

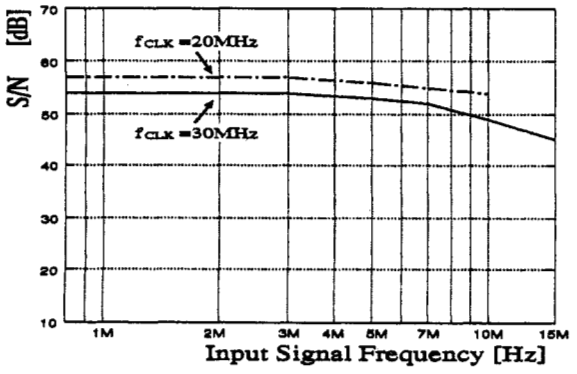

Figure 8. Input signal frequency vs. S/N
(0 dB full scale input, Vcc=1.5 V)

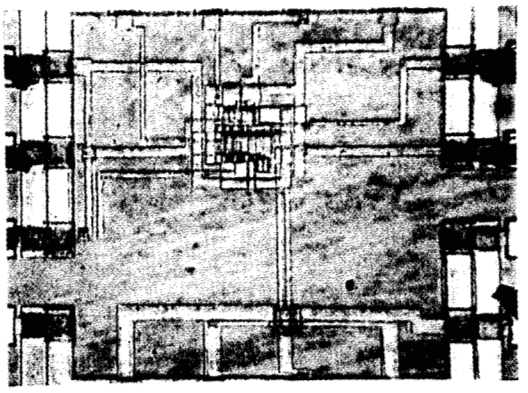

Figure 9. Microphotograph of the chip

Table 1. Overall chip performance

Item		Value	Unit
Vcc		1.5	V
S/N			
1MHz , clock 30MHz		54	dB
15MHz , clock 30MHz		45	dB
1MHz , clock 20MHz		57	dB
Distortion 1MHz input 2nd clock 30MHz		-48	dB
Power dissipation		2.3	mW
Process		CMOS 0.6um	
Vth	NMOS	+0.7	V
	PMOS	-0.7	V