THE DESIGN OF A 1V, 40MHZ, CURRENT-MODE SAMPLE-AND-HOLD CIRCUIT WITH 10-BIT LINEARITY

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ABSTRACT

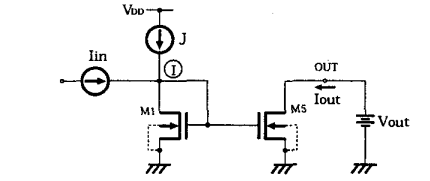
We designed a 1V, 40MHz current-mode sample-and-hold circuit with 10-bit linearity and simulated its circuit using the parameters from CMOS 0.6μm low-threshold voltage (low V_{th}) transistors. A new current mirror circuit with low input impedance and low-voltage operational capability was developed. Feed-through errors generated by the sample switches were effectively canceled by the differential placement of switches at inputs of a differential amplifier. The boosted voltage was generated and applied to the gate of sample switches to make their on resistances low. The simulation resulted in a 1.9mW power dissipation, 10-bit linearity error for an input signal frequency of 1 to 8MHz, an input current of $\pm 200\mu$A, a clock frequency of 40MHz, and a supply voltage of 1V.

1. INTRODUCTION

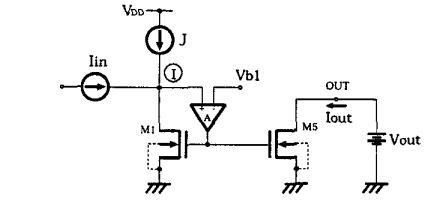
The coming personal and mobile communications era requires LSIs that operate using a low supply voltage to achieve low power consumption. The supply voltage reduction, therefore, becomes an urgent problem to be solved for analog circuits in the near future [1]. This paper investigates the possibility of analog devices which operate at supply voltages as low as 1V by adopting a current-mode approach. The designed and simulated example is a 40MHz, 10-bit level current-mode sample-and-hold circuit operating from a 1V supply.

2. A NEW LOW-VOLTAGE, HIGH-PERFORMANCE CURRENT MIRROR CIRCUIT

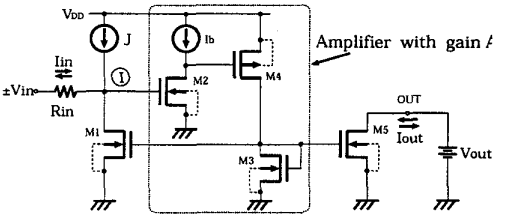
The current mirror circuit is dominant in the current-mode approach. Figure 1(a) shows a conventional MOS current mirror circuit which is capable of operating with a 1V power supply [2]. In this configuration, the drain or gate voltage of M1 changes when input signal



(a) Conventional low-voltage current mirror circuit



(b) Conceptual low-voltage, highly accurate current mirror circuit



(c) Actual low-voltage, highly accurate current mirror circuit

Figure 1: Low-voltage current mirror circuits

current I_{in} changes. The voltage change at terminal I (ΔV_{Icon}) becomes

$$\Delta V_{Icon} = \frac{I_{in}}{g_{m1}} \quad (1)$$

where g_{m1} is the transconductance of M1. This causes the drain-to-source voltage of M1 to differ from that of M5. As a result, a current mismatch between I_{in} and output current I_{out} is introduced. There is another error source in the circuit in Fig.1(a). When V_{out} changes, I_{out} changes due to the finite output re-

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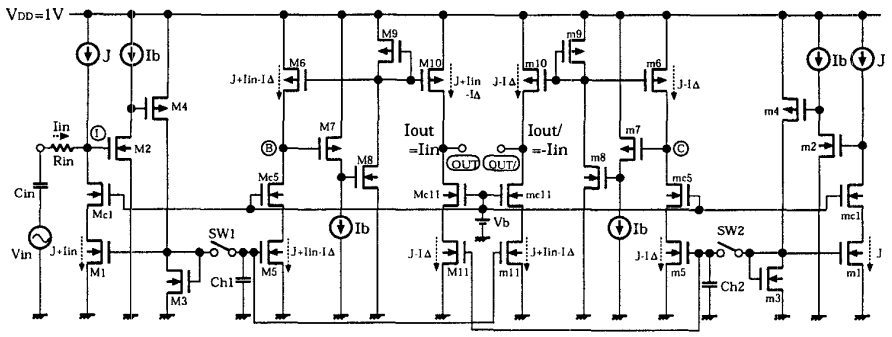

Figure 3: Complete differential sample-and-hold circuit

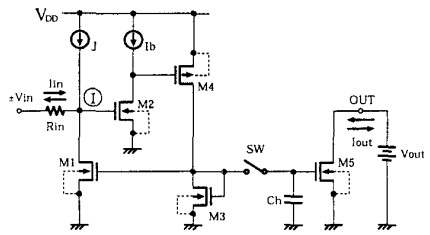

Figure 2: Realization of the current-mode sample-and-hold circuit

sistance of M5. Figure 1(b) shows a circuit that can suppress the voltage change at terminal I. The voltage change ΔV_{In} at terminal I is suppressed by the gain A of the op-amp and becomes

$$\Delta V_{In} = \frac{I_{in}}{A \cdot g_{m1}} \tag{2}$$

As voltages at both terminals I and OUT become constant in Fig.1(b), accurate current mirror operation is achieved. Figure 1(c) realizes the circuit shown in Fig.1(b) for supply voltages as low as 1V. Transistors M2, M3, M4, and a constant current source I_b form a positive amplifier. The voltage at terminal I is now fixed, and Signal current is applied through the resistor R_{in}.

The minimum supply voltage of the circuit in Fig.1(c) becomes $V_J + V_{DSM1}$, $V_{Ib} + V_{DSM2}$ or $V_{DSM3} + V_{DSM4}$, where V_J and V_{Ib} are voltages necessary for maintaining constant current sources and V_{DS} is the drain-to-source voltage of a transistor. To a first order approximation, they all become $V_{th} + 2\Delta$, where V_{th} is the threshold voltage of a transistor and the Δ is the minimum voltage necessary to keep transistors in saturation. The minimum supply voltage is calculated as less than 1V for the Δ of 0.3V and the V_{th} of less than 0.4V.

3. SAMPLE-AND-HOLD CIRCUIT DESIGN

The circuit in Fig.1(c) can be extended to perform the sample-and-hold function by placing an analog switch (SW) and a hold capacitor C_h between M3 and M5 as shown in Figure 2. When the analog switch turns on, I_{out} is the exact copy of the input signal current plus the constant current J. When the switch opens, the gate-to-source voltage of M5 is memorized in C_h and I_{out} becomes constant. Only one analog switch was used in the circuit in Fig.2. When we consider the accuracy, we should use the minimum number of small analog switches in the circuit because the feed-through error from switches greatly reduces the accuracy. In this sense, the circuit in Fig.2 generates less feed-through, however, the switch's on-resistance dependence on the signal level, together with the hold capacitor, causes fluctuation in the RC time constant and deteriorates the high-frequency characteristic of the circuit. Some means to reduce the switch's on-resistance is needed. We used a higher voltage than the supply for the gate of the switching transistor by boosting the voltage.

The designed 1V operational sample-and-hold circuit is shown in Fig.3. The circuit has a differential configuration and symmetrical halves. The input signal V_{in} is converted from voltage to current through the capacitor C_{in} and resistor R_{in}, and is applied to terminal I. Transistors M1 through M5, SW1 and C_{h1} form the sample-and-hold circuit as shown in Fig 2. An identical circuit (m1 through m5, SW2 and C_{h2}) is prepared to cancel the switch feed-through error by using the differential configuration [3]. Transistors M6 through M10 or m6 through m10 are the PMOS based version of the circuit in Fig.1(c). The voltage at terminals B and C becomes constant, and the current mirror ratio between M1 and M5 (m1 and m5) is accurate. The identical circuit is utilized to produce the I_{out}/ signal. The current $J + I_{in}$ flows through M5, M6,

M10 and m11 when SW1 turns on. Since the current J flows through M11, m5, m6, and m10, $+I_{in}$ and $-I_{in}$ are obtained at Out and Out/ terminals, respectively. The current error due to switch feed-through which is expressed as I_Δ, is also shown in Fig.3. The figure indicates that the I_Δs cancel each other. The current mirror transistors are connected in a cascode configuration because their output impedances still change as signal current changes.

4. GATE VOLTAGE BOOSTING CIRCUIT

To reduce the on-resistance of a switching transistor, we can boost its gate voltage. Figure 4 shows the gate-voltage boosting circuit. Our 0.6μm CMOS process allows the bulk terminal of only a PMOS transistor to be tied to any desirable voltage, which is commonly the supply voltage. When the CLK IN terminal becomes high, transistors M2, M3, M4 and M6 turn on. The voltage at terminal A then becomes zero (ground potential), and the voltage at terminal B becomes $V_{DD} - \alpha$. Here, α is the voltage difference between drain and source of the low V_{th} transistor M4 and is 0.2 to 0.3V. Though the bulk of M4 is connected to its drain, there is no leakage current from source or bulk to the substrate. Capacitor C is charged to $V_{DD} - \alpha$. When the CLK IN terminal becomes low, transistors M1 and M5 turn on, and all other transistors turn off. As the voltage at terminal A swings to V_{DD}, the voltage at terminal B swings to $2V_{DD} - \alpha$. In the conventional configuration without M4, the maximum voltage at terminal B is limited to $2V_{DD} - V_b$, where V_b is the forward voltage of a drain-to-bulk pn-junction diode which is a parasitic device of M3. M4 in Fig.4 prevents this situation. Both the source-to-bulk and the bulk-to-substrate pn-junction diodes become reverse-biased when the voltage at B rises above V_{DD}. The voltage at B is expected to be about 1.7V when V_{DD} is 1V and α is 0.3V, while it is only 1.3V for the conventional configuration where V_b is 0.7V. The bulk terminal of M5 is tied to its source instead of V_{DD} so that no leakage current flows and the voltage at B is not reduced.

5. SIMULATION RESULTS

The designed circuit was SPICE simulated by using 0.6μm MOS device parameters. The V_{th} of an NMOS transistor is 0.24V and that of a PMOS transistor is -0.20V. Figure 5 shows the difference error current between I_{in} and I_{out} for circuits in Fig.1(a) and Fig.1(c). The constant current J is excluded. The absolute current error reaches 100μA for the circuit in Fig.1(a)

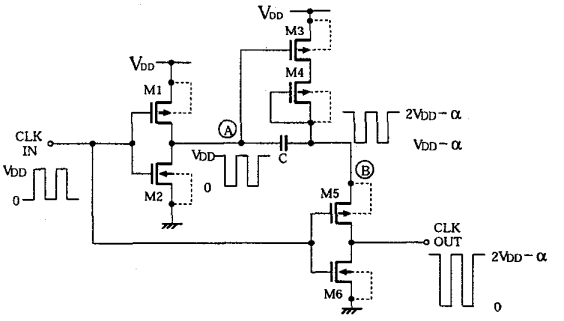

Figure 4: Gate voltage boosting circuit

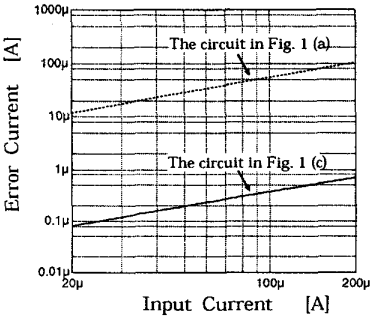

Figure 5: Difference error current between I_{in} and I_{out} for circuits in Fig.1(a) and Fig.1(c)

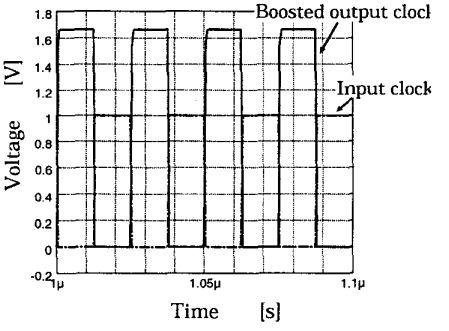

Figure 6: Sampling clock waveform at the gate of the switch

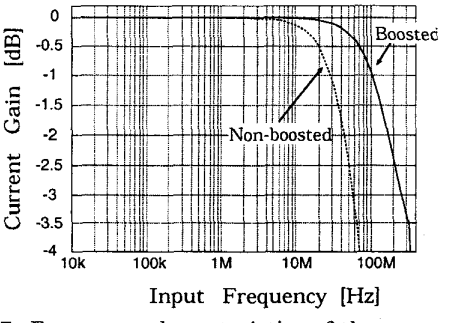

Figure 7: Frequency characteristics of the current gain in sample mode

when I_{in} is 200μA. If the curve in Fig.5 were completely linear, then the error would not affect the linearity or distortion on the output signal. Instead, it would cause a gain error. However, this is not the case in Fig.5. It is therefore not completely linear, so it is better to minimize the error. The circuit in Fig.1(c) has less than 0.5% of absolute current error.

In Fig.3, I_{in} is $\pm$200μA peak-to-peak, and J and I_b are 225μA and 50μA, respectively. SW1 and SW2 are composed of an NMOS transistor with a W of 4μm and L of 0.6μm together with a half-size feed-through compensation transistor. C_{h1} and C_{h2} are 0.3pF, and the supply voltage V_{DD} is 1V. C in Fig.4 is chosen to be 2pF. The estimated total power dissipation is 1.9mW.

Figure 6 shows the waveform at the gate of the sampling switch in Fig.3 when a 40MHz clock is applied. The voltage is effectively boosted to 1.65V.

Figure 7 shows the frequency characteristics of the current gain when the circuit is in the sample mode. The input was $\pm$200μA peak-to-peak, and either the output current I_{out} or $I_{out}/$ was taken as the output. A 3dB frequency bandwidth of 250MHz was obtained when the boosted gate voltage (1.65V) was used. In the figure, the frequency characteristics with a non-boosted gate voltage (1V) are shown for comparison. Its 3dB frequency bandwidth was only 60MHz.

Figure 8 shows the input and output current characteristics in the sample-and-hold mode with a 40MHz clock and 2MHz input signal. $I_{out} - I_{out}/$ was taken for the output, and the peak-to-peak current became 800μA. The input current was $\pm$200μA, and it was doubled arithmetically to overwrite in the figure. The 0.4μA error current becomes the half-bit equivalent error for 10-bit accuracy during differential operation. The figure displays the maximum of 0.514μA of error current for the various current steps included in the rising edge of the input, and 0.425μA in the falling edge. The influence of clock feed-through was almost completely eliminated.

Figure 9 further simulates the linearity up to the input frequency of 10MHz. When a non-boosted gate voltage is applied, the error becomes large as signal frequency increases. In contrast, when a boosted gate voltage is applied, the frequency error remains below 0.1% up to 8MHz.

6. CONCLUSION

Clearly, a current-mode MOS sample-and-hold circuit with a 40MHz clock, 10-bit accuracy, and operation from a 1V power supply is feasible.

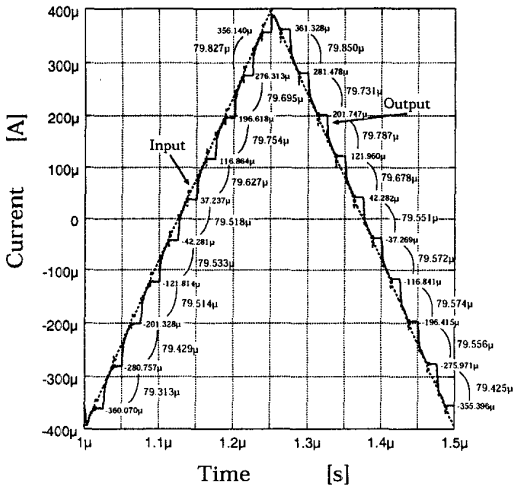

Figure 8: Input and output current characteristics in the sample-and-hold mode

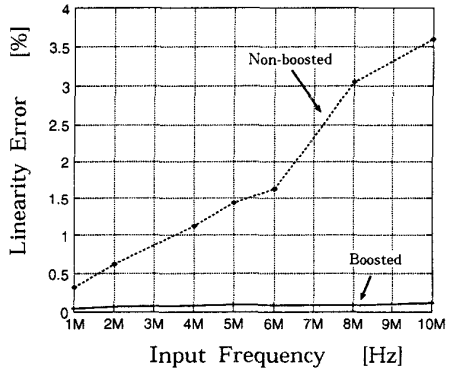

Figure 9: Frequency characteristics of the linearity error

7. REFERENCES

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