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A 2 V, 500 MHz and 3 V, 920 MHz Low-Power Current-Mode 0.6 μm CMOS VCO Circuit

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SUMMARY This paper describes an MOS current-mode, voltage-controlled oscillator (VCO) circuit that potentially operates with a 2 V supply voltage, 500 MHz oscillation frequency, and −90 dBc/Hz phase noise at the 1 MHz offset. It also has an improved oscillation frequency linearity of the control voltage and 11 mW power dissipation. The oscillation frequency reached 920 MHz when the supply voltage was increased to 3 V.

key words: *low voltage, high frequency, high performance, MOS analog, VCO*

1. Introduction

Supply voltages, especially for logic LSIs, are rapidly decreasing to 1 to 2 V. Most current high-speed logic LSIs, such as microprocessors, incorporate a phase locked loop (PLL) function to synchronize the internal flip flops with a clock. Therefore, a very high-speed PLL that operates at 1 to 2 V is required. The key element in the PLL is the VCO. We believe that using a current-mode circuit is promising approach for realizing the required function in the near future. This paper examines whether a CMOS VCO can be realized by utilizing a current-mode approach and whether the supply voltage can be reduced while preserving high-frequency capabilities. The possibility of operating a near-gigahertz VCO at 1 V is also discussed.

2. Low-Voltage, Low-Power, High-Frequency Operation with Improved Linearity

A ring-oscillator type VCO is preferable for constructing a PLL in a logic LSI. The block diagram of the designed VCO is shown in Fig. 1. It is very similar to that in Ref. [1], but differs in that current-based amplification is done throughout the circuit and in that two delay cells compose one delay block. In order to achieve low-voltage and low-power characteristic, new delay cells in a ring-oscillator type VCO, whose output voltage swing is suppressed, were designed based on the current-mode circuit technique as shown in Fig. 2. This figure shows two delay cells, A5 and A6, connected in series. At the transition of A5 outputs, a current change of $+\Delta I$ ($-\Delta I$) occurs in Mp51 (Mp52). As a result, the voltage change $\Delta I/g_{mp}$, where g_{mp} is the transconductance of a PMOS load transistor, occurs across each load in opposite directions. This voltage change is then applied to the gates of NMOS differential pair Mn61 and Mn62 in A6. The current change $+\Delta I'$ and $|-\Delta I'|$ in A6 then becomes $(g_{mn}/g_{mp}) \times \Delta I$, where g_{mn} is the transconductance of an NMOS transistor, thus amplifying the current. The voltage swing for A5 outputs is small. In calculating the minimum supply voltage ($V_{DD_{min}}$) of a delay cell in Fig. 2, we assume the same threshold voltage (V_{th}) for both the PMOS and NMOS transistors. We also assume that the transistor requires $\Delta = \sqrt{2I/\beta}$ for drain-to-source voltage to keep it in saturation, with I being the current flowing through a transistor, and β, the transconductance parameter. $V_{DD_{min}}$ is then calculated as

$$V_{DD_{min}} = 2V_{th} + 2\Delta \tag{1}$$

When $V_{th} = 0.8$ V and $\Delta = 0.25$ V, $V_{DD_{min}}$ becomes 2.1 V. It is clear that the minimum supply voltage depends heavily on V_{th} because the influence of the output voltage change is largely reduced. If we could reduce V_{th} to 0.25 V, the circuit could operate at 1 V.

Next, we increased the oscillation frequency by combining the current transitions at outputs of delay cells A1, A3 and A5. Figure 3 shows the output current wavesforms from the Gm cells in Fig. 1. Currents from Gm cells (I1, I2/ and I3) are combined and become the current I1+I2/+I3 as shown in the figure. In this case, the final oscillation frequency becomes three times

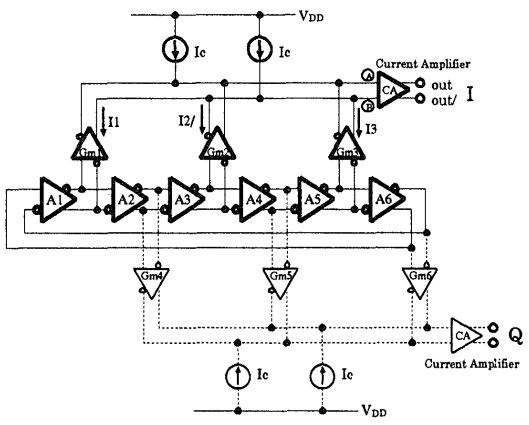

Fig. 1 Block diagram of the designed VCO.

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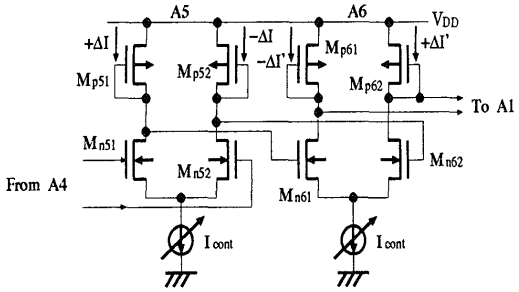

Fig. 2 Low-voltage and low-power realization scheme. (Use of current-mode delay cells)

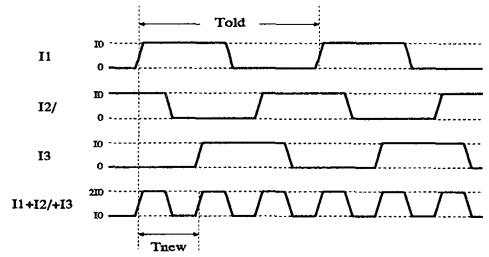

Fig. 3 High-frequency realization scheme. (Combined output generation)

higher than that of a ring oscillator. A quadrature-phase output can easily be obtained by combining the current outputs of delay cells A2, A4 and A6 in the same manner as indicated by the dotted lines in Fig. 1 [2]. This is why every two delay cells are used as a delay block. Unfortunately, the quadrature-phase output generation function was not provided on the chip fabricated this time.

The propagation delay time of a delay cell, *tdcell*, is calculated as

$$tdcell = (C_s/g_{mp}) \ln 2 \tag{2}$$

where $g_{mp} = \sqrt{2\beta_p \times I_{cont}}$, C_s is the sum of the stray capacitance, and β_p is the transconductance parameter of a PMOS load transistor. This is shown in Fig. 4. If we cannot decrease the number of delay cells to achieve three times higher oscillation, Eq. (2) implies that we need a current nine times greater than I_{cont} for a cell. It is clear that the current combination technique adopted here also results in low power. Transconductance g_{mp} becomes proportional to the root of I_{cont} in Fig. 4, and the load resistance becomes inversely proportional to V_{cont} (VCO control voltage) minus V_{thn}, where V_{thn} is the V_{th} of an NMOS transistor. I_{cont} is generated by the circuit shown in Fig. 5. In the figure, Mn22 operates in the saturation region and Mn21 and Mn3, and Mp21 and Mp22 form current mirror circuits. V_{cont} is applied to the gate of Mn22 and produces a drain current proportional to the square of V_{cont} minus V_{thn}. The drain current is then mirrored and finally becomes I_{cont}. As the oscillation frequency of the VCO (f_{VCO}) is caculated as

$$f_{VCO} = 1/(2N \times tdcell) \tag{3}$$

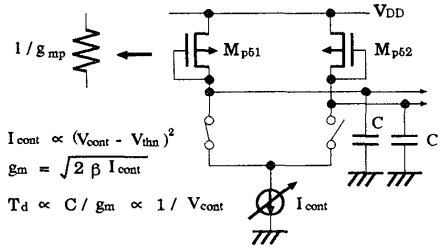

Fig. 4 High-performance realization scheme.

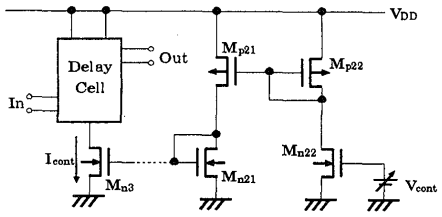

Fig. 5 Delay control circuit.

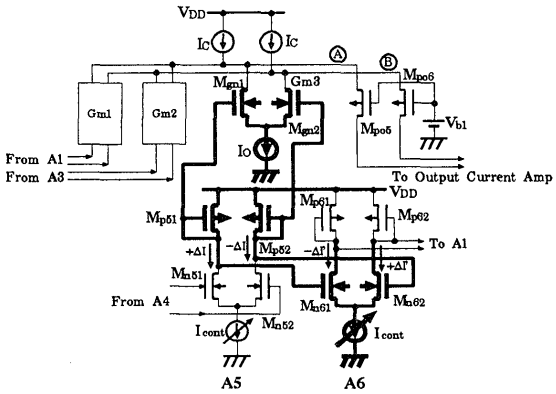

Fig. 6 Delay cell and Gm cell circuit.

where N is the number of delay cells, linearity is expected between the oscillation frequency and V_{cont} minus V_{thn}.

3. VCO Circuit Design

Figure 6 shows a portion of the circuit. A5 and A6 are delay cells; Gm1, Gm2 and Gm3 are voltage-to-current converters in Fig. 1. PMOS loads in A5 and a differential NMOS pair in A6 amplify the current. The same kind of current-to-current conversion is performed by PMOS loads in A5 and a differential NMOS pair in Gm3, whose tail current is the constant value I_o. The combined current of Gm1, Gm2 and Gm3 is then compared to the constant current I_c, and the difference current flows in Mpo5 and Mpo6 to become currents for further amplification by the output current amplifier. Since a sufficient current change cannot be obtained in the current composition stage, especially at high frequency, it is necessary to amplify the current more in the latter stage. Refer to Ref. [3] for circuits of the current amplifier.

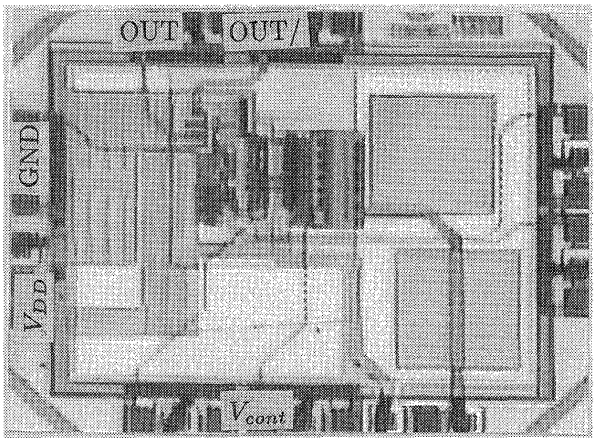

Fig. 7 Photograph of the chip.

The circuit simulation suggests that the designed VCO could operate at 1 GHz with a 1 V supply if low V_{th} transistor of 0.25 V are used and I_{cont} value is increased [3].

4. Experimental Results

The VCO was fabricated using the standard CMOS 0.6 μm process. Figure 7 shows a photogragh of the test chip. The threshold voltages (V_{ths}) of the transistors were +0.8 V for NMOS and −0.8 V for PMOS. Figure 8 indicates the linear relationship between the oscillation frequency and the control voltage. The measured and SPICE-simulated data agreed well. The oscillation frequency in the figure was obtained for a V_{DD} of 3 V with V_{cont} varying from 1.3 V to 3 V. When V_{cont} was 2 V, the oscillation frequency was 500 MHz; when V_{cont} was increased to 3 V, it reached 920 MHz. When the VCO was operated with a 2 V supply at an oscillation frequency of 500 MHz, the measured I_{cont} and I_o values in Fig. 6 were 130 μA and 185 μA, respectively. In this case, the total power consumption, excluding that of the output current amplifier, becomes about 4 mW. The output current amplifier needs 7 mW more power. Figure 9 shows the VCO spectrum at an oscillation frequency of 500 MHz for V_{DD} of 2 V. The phase noise at the 1 MHz offset was −90 dBc/Hz. The previous work on a VCO1 circuit in Ref. [4] reported an oscillation frequency of 300 MHz with a 2 V supply, and phase noise of −83 dBc/Hz at 100 kHz offset with a 5 V supply and nonlinear control characteristics of the oscillation frecuency. It should be necessary to improve the phase noise by 10 dB in our work. However, high-frequency oscillation and linear control characteristics of the oscillation frequency while operating with a low supply voltage are useful for clock generation PLLs in various logic circuits.

5. Conclusions

We verified the ability of current-mode circuits to realize a low-voltage, low-power and high-frequency CMOS VCO by designing, fabricating, and evaluating a same circuit. Our analysis implies the possibility of a 1 V operational VCO in the near future.

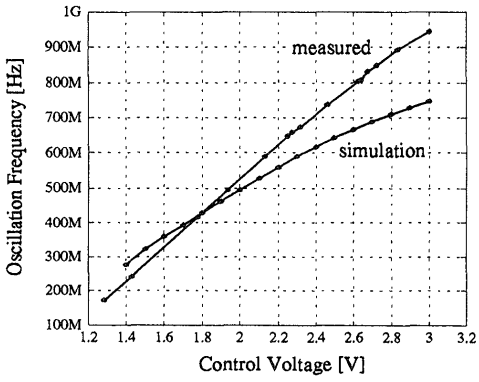

Fig. 8 Control voltage vs. oscillation frequency characteristics.

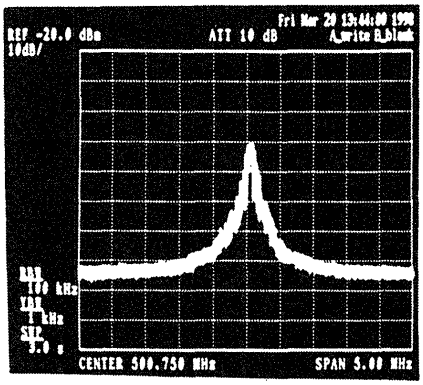

Fig. 9 Spectrum of the output signal.

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