A Low-Voltage, High-Speed and Low-Power Full Current-Mode Video-rate CMOS A/D Converter

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This paper examines the feasibility of developing a full current-mode video-rate CMOS A/D converter (ADC), with 1V operation in mind in the future. The initial specification in the design stage was resolution greater than 8-bits, 20MHz clock frequency and 40mW of power dissipation from a 3V power supply. A fully current-mode pipeline ADC was created by using 0.6 μm CMOS process, resulting in 7-bit equivalent S/N, 20MHz clock speed, 3V operation and 100mW of power dissipation. It indicates the possibility of realizing a low-voltage video-rate ADC by using the full current-mode circuit approach.

1. INTRODUCTION

The supply voltage of LSIs will probably decrease to 1V in the near future. High-performance, low-power, low-cost and small-size portable equipment will be realized with this supply voltage. From an LSI implementation point of view, operating at such low voltage is easier for digital circuits than for analog circuits. Among various analog circuits, a video-rate ADC is one key function to be realized with this low supply voltage. The current mode approach for low-voltage, high-performance analog operation is promising. Although several current-mode ADCs have been developed, they have not achieved high-speed [1,2], low voltage [3], and full current-mode operation [4]. We believe the first step toward a 1V video-rate ADC in the future is to verify the performance of a full current-mode ADC in terms of 20MHz operational capability and resolution greater than 8-bits with lower supply voltage. For this paper, we investigated the feasibility of producing a pipeline full current-mode CMOS ADC through the design, fabrication and evaluation of an actual chip. The details are described below.

2. PIPE-LINED FULL CURRENT-MODE ADC CIRCUIT

The ADC consists of pipeline 1.5-bit bit-blocks with a 20MHz differential current-mode

sample-and-hold circuit and a 1.5-bit current-mode bit-cell circuit, as shown in Fig. 1. We used a digital correction scheme, but no calibration technique. Employing a high-speed sample-and-hold circuit enables each bit-block to operate in clock speed. Here, the key issue was creation of a 20Mz and 8- to 10-bit level sample-and-hold circuit unaffected by switch feed-through error and poor transistor output impedance. Precise matching of current mirror transistors is crucial to obtain good differential nonlinearity and integral nonlinearity characteristics in the current-mode ADC. Figure 2 shows a new sample-and-hold circuit which eliminates the switch feed-through error. Analog switches were placed differentially between the input current to voltage (I-V) converter and the output differential amplifier. The circuit is configured such that two basic current mirrors with analog switches are connected in parallel. For analog switches, low on-resistance is required to achieve high-speed operation. Transistors with low threshold voltage (Vth) can be used in this configuration since the DC voltage of analog switches was kept at VDD/2. Therefore, it is not necessary to consider the sub-threshold leakage current of a switch transistor. The error caused by switch feed-through was canceled by the common-mode rejection characteristics of the differential amplifier. The minimum supply voltage required for the circuit operation is calculated as $2(Vth+2\Delta)$, where $\Delta=\sqrt{2I/\beta}$, I is the current which flows through a transistor and β is the transconductance parameter. Vth can be set to 0V in this configuration to enable the 1V operation; however, this is left for future study. A cascode connection of the transistors was used throughout the circuit to increase the transistors' output impedance. Figure 3(a) shows the schematic of the 1.5-bit bit cell circuit; Fig. 3(b) shows the input current versus output current characteristics of the bit-cell. The bit-cell consists of a 1.5-bit ADC, DAC and current subtraction circuit. The input current was doubled and applied to current comparators. Comparison speed is fast enough because the line equalization technique is used in a latch circuit. The output current, Iout, becomes the difference current between the doubled input current and the DAC currents. Two equal current sources are prepared for the DAC. The analysis says the Vth variation of transistors in these current sources should be less than 3mV to achieve 8-bit resolution. The minimum supply voltage for the 1.5-bit bit cell circuit is calculated to $2Vth+3\Delta$, and this is lower than that of a sample-and-hold circuit. The cascode connection of the transistors was also retained.

3. EXPERIMENTAL RESULTS

The designed circuit was completed and evaluated. The transistor Vth was +0.9V for NMOS and -0.9V for PMOS; the switch transistors had Vths of +0.4V for NMOS and -0.4V for PMOS. Although the chip was initially designed in a 10-bit configuration with an input current of $\pm 20\mu$A, a poor S/N was observed in the first stage of evaluation. Therefore, the input current value was increased to $\pm 50\mu$A when the ADC was evaluated. With this increase, the current in the remaining circuits was automatically increased by 2.5 times. However, this is not constant. By changing the design a little bit, the current consumption can be kept almost equal. It was possible to evaluate a sample-and-hold circuit separately. In this case, the input current could be increased to $\pm 110\mu$A with a 3V supply voltage. Figure 4 shows S/N versus input signal frequency characteristic. The upper curve is S/N measured with 10MHz bandwidth in sample mode; the lower is that in sample-and-hold mode. Clock speed is 20MHz. 57dB of S/N was obtained in sample mode. This is lower than our expectation. Since the signal voltage is suppressed in the current-mode circuit, it is turned out that only a limited S/N value is obtained. S/N of 50 to 51dB was obtained in sample-and-hold mode. Though the input current can only

be increased to $\pm 50\,\mu$ A in this ADC evaluation, the data in Fig. 4 indicates that an equivalent S/N of 8 bits or more can be obtained if the input current is increased. The ADC evaluation was conducted by reconstructing the signal using a 10-bit video-speed bipolar DAC. Figure 5 shows the S/N versus the input signal level. The input frequency was 1MHz, the supply voltage (VDD) was 3V, and the clock frequency was 20MHz. A S/N of 42dB measured with 10MHz bandwidth, equal to a 7-bit equivalent performance, was obtained. This is coincident with the result in Fig. 4. As input current is reduced from $\pm 110\,\mu$ A in Fig. 4 to $\pm 50\,\mu$ A in Fig. 5, about 7dB degradation of S/N occurs. Figure 6 shows the S/N dependency on the input signal frequency with a full-scale input level. The S/N degraded when the input frequency exceeded 1MHz even though a sample-and-hold circuit is placed at the input of the ADC. This should be further investigated. Figure 7 shows the differential nonlinearity error. 1LSB corresponds to 8-bit level resolution. Less than $\pm$1LSB of differential nonlinearity error was observed. Figure 8 shows the output spectrum with a full-scale input signal. The third harmonic level was the largest at -36dB of full-scale, while the second harmonic level was -44dB. Those harmonic levels decrease when the input level decreases. Figure 9 is a chip photograph. The die size is 3x4 mm^2.

4. CONCLUSION

A full current-mode pipe-lined ADC was designed, created, and evaluated to examine the feasibility of use in future low-voltage analog circuits. The resulting performance was 20MHz, 3V, with a 7-bit equivalent S/N, and 100mW of power dissipation in a 10-bit configuration. This is the first full current-mode ADC that has achieved 20MHz operation. It indicates the possibility of an 8-bit level of low-voltage video-rate ADC in the future.

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[4] M.Yotsuyanagi, et al., " A 2V 10b 20MSample/s Mixed-Mode Subranging CMOS A/D Converter ", ISSCC Digest, pp.282-283, February 1995.

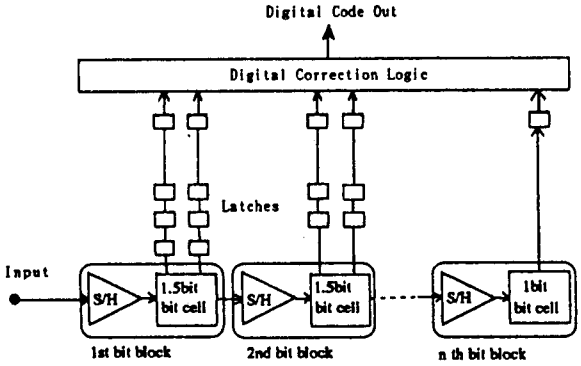


Fig. 1 New pipe-lined ADC architecture

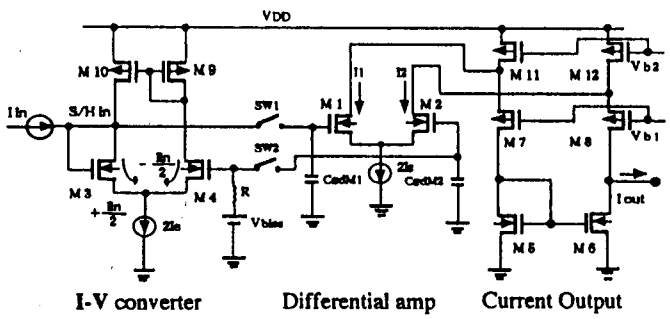
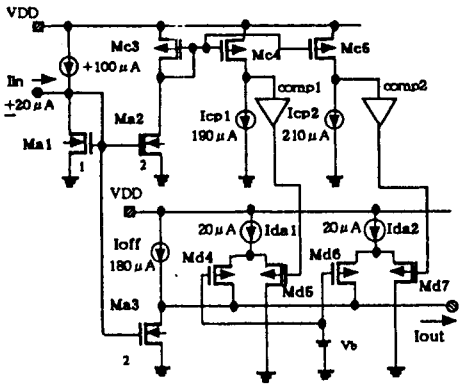
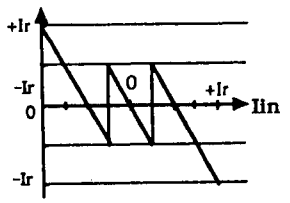


Fig. 2 Schematic of a sample-and-hold circuit



(a) Schematic of the bit-cell circuit



(b) Input vs. output current characteristic

Fig. 3 1.5-bit bit cell circuit

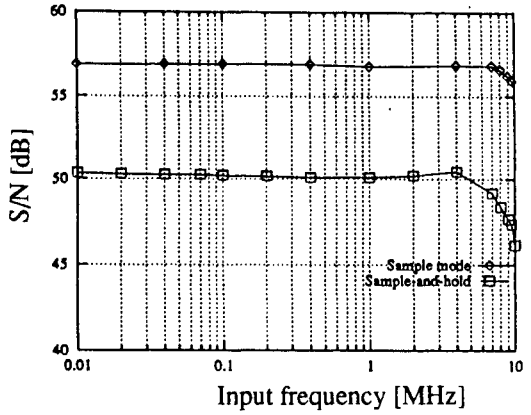


Fig. 4 S/N vs. input frequency of a sample-and-hold circuit (3V, 20MHz, Iin=$\pm$110μA)

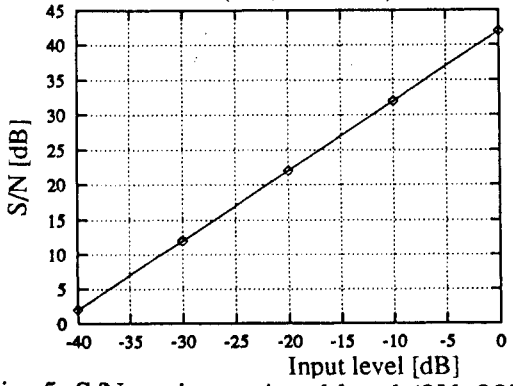


Fig. 5 S/N vs. input signal level (3V, 20MHz, fin=1MHz, full scale=0dB)

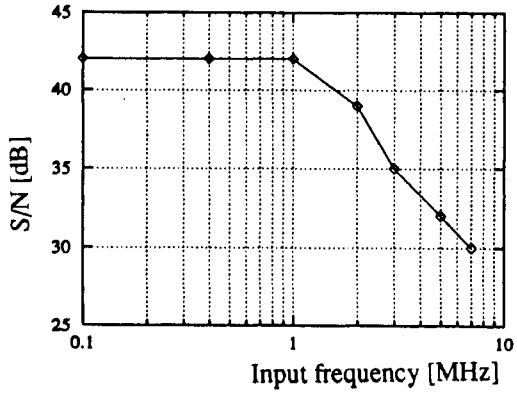


Fig. 6 S/N vs. input signal frequency (3V, 20MHz, full scale input)

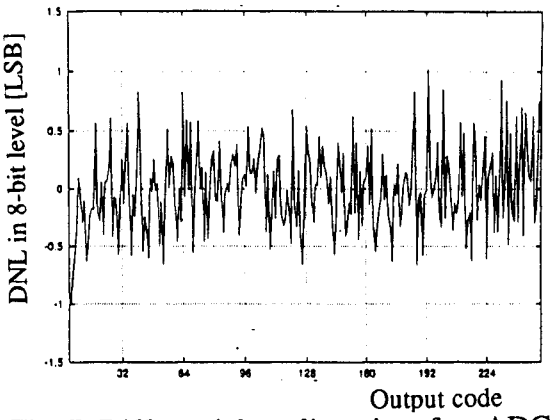


Fig. 7 Differential nonlinearity of an ADC

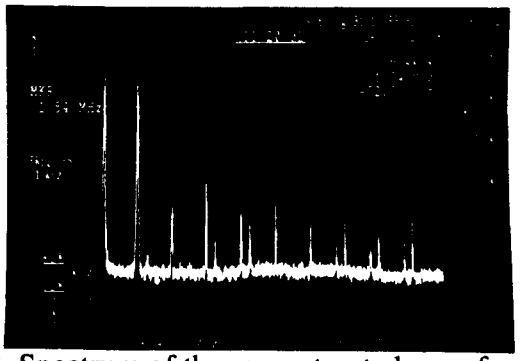


Fig. 8 Spectrum of the reconstructed waveform (3V, 20MHz, fin=1MHz, H:1MHz/div, V:10dB/div, RBW=10kHz, VBW=300Hz)

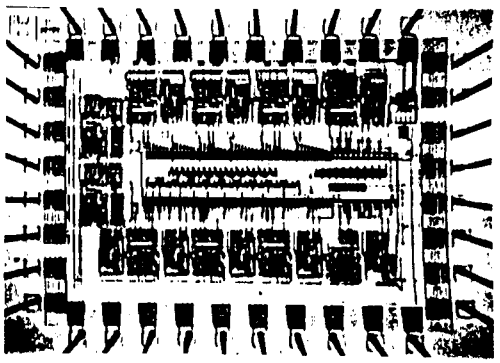


Fig. 9 Chip photograph