The Design of a 1V, 1GHz CMOS VCO Circuit with In-phase and Quadrature-phase Outputs

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Abstract

A CMOS ring-oscillator type VCO circuit with in-phase (I) and quadrature-phase (Q) outputs has been designed by using 0.6 μm MOS devices. This VCO has demonstrated 1V and 1GHz operational capabilities. Two differential delay cells has been used as one delay section and the transitions of the delay cell outputs have been combined, and thus the 1GHz I/Q output generation has been realized. The current-mode approach throughout the design has resulted in the extremely low voltage operation. The simulation results show more than 1.4GHz oscillation frequency from a 1V power supply, and less than $\pm 1^\circ$ phase error for I/Q outputs when Vth variation is 10mV.

1. Introduction

Emerging mobile and portable communication equipments require high-frequency analog circuit to operate with extremely low voltage and low power. In addition, a system-on-a-chip LSI, which is composed both of high-frequency analog and of a large size of logic circuits, is also required. The use of the unified LSI process, such as CMOS, becomes inevitable. We have tried to design a CMOS VCO circuit, which operates at more than 1GHz oscillation frequency from a 1V power supply. Especially, a VCO for a communication equipment requires both I and Q outputs. [1] Therefore, the effective way of generating I/Q outputs in a ring-oscillator type CMOS VCO is examined at first in chapter 2. Next, the circuit design of each block in the VCO that realizes low voltage operation will be described in chapter 3. Chapter 4 shows the SPICE simulation results, and chapter 5 concludes the paper.

2.The I/Q output generation at 1GHz

Amplitude and phase errors of I/Q signals need to be less than 1dB and $\pm 1^\circ$, respectively. Figure 1 shows the conventional phase shifter circuit that utilizes resistors and capacitors. [2] The components' mismatch generates unacceptable errors to the amplitude and phase of I/Q signals. Figure 2 shows the simple way to produce I/Q signals in a ring-oscillator type VCO. [1] As a ring-oscillator is composed of four delay cells, the time interval of one cycle of oscillation becomes 8td, where td is the delay of a delay cell. By taking out the outputs as shown in the figure, we can obtain two output waveforms that differ each other by 2td, i.e. $\pi/2$ in phase. In this case, however, the oscillation frequency becomes 1/8td, and is very low. High frequency oscillation is still available even when a ring-oscillator type VCO is used, by combining transitions of each delay cell output as shown in Fig. 3. [3] Each delay cell output voltage is converted into current by a gm cell and is added up to determine a single output current. The resulting output current changes three times faster than the original ring-oscillator's voltage.

The effective way to obtain high-frequency I/Q output signals is developed by combining these ideas. Figure 4 shows the block diagram of the newly developed VCO circuit and Fig. 5 shows waveforms observed at different places of the circuit. Six differential-type current-mode delay cells, from A1 to A6, consist of a ring-oscillator, whose oscillation period (Told) is 12td, where td denotes the delay of one delay cell. Again, a gm cell converts the voltage change at each delay cell output into current. Then, I signal becomes the addition of currents I2, I4/ and I6, and Q signal becomes the addition of currents Q1, Q3/ and Q5. As can be seen in Fig. 5, the oscillation period Tnew of the waveform I or Q becomes one-third of the original currents, that is 4td. This is two times faster than the oscillation interval in Fig. 2. Assuming that the time delay of all gm cells is equal, I2 in Fig. 5 becomes the inverted version of Q1 with the time delay of td. In the same way, I4/ and I6 become the inverted versions of Q3/ and Q5, respectively, with the time delay of td. As a result, I output becomes the inverted version of Q output with time delay of td. This means Q delays $\pi/2$ in phase relative to I. By adopting the configuration shown in

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Fig. 5, we can obtain high-frequency I and Q outputs while making oscillation frequency of the ring-oscillator low. The $\pi/2$ phase difference doesn't change regardless of the ring-oscillator frequency.

3.The VCO circuit with low voltage operational capability

The detailed VCO circuits are shown from Fig. 6 to Fig. 8. Fig. 6 is the delay cell and the control circuits. The delay cell is composed of a simple input differential pair (MN1 and MN2) with diode-connected load transistors (MP1 and Mp2) and a current source transistor (MN3). In this configuration, the equivalent resistor of a load transistor is 1/gm, where gm is the transconductance of a PMOS transistor. As the gm is proportional to the square root of the control current source Icont flowing in MN3, the equivalent load resistor value is inversely proportional to Vcont (VCO control voltage) if Icont is controlled to be proportional to the square of Vcont. As the VCO oscillation frequency is the inverse of the time constant at loads, the linear relationship between oscillation frequency and Vcont is obtained.

The low voltage operation is important for this VCO. The minimum operating supply voltage is evaluated. First, assume the same threshold voltage Vth for both PMOS and NMOS transistors, and further assume that a transistor needs $\Delta=\sqrt{2I/\beta}$ for drain-to-source voltage to keep it in saturation, where I is the current flowing through a transistor and β is the transconductance parameter. Then the minimum supply voltage VDDminc becomes;

$$VDDminc=2Vth+2\Delta \quad (1)$$

When Vth=0.2V and Δ=0.25V, VDDminc is 0.9V. Figure 7 shows the circuit to generate the combined output current. MN51, MN52 and MN53 consist of a gm cell, and it converts the voltage change at inputs into the current change. MN53 is the constant current source. The output of each gm cell is connected together, and the difference current between the constant current source Ic (MPO2 or MPO3) and the combined output current is applied to the A or B terminal. Figure 8 shows the output circuit. The current change at terminals A and B is small especially at high frequency, and it needs to be amplified to interface to other circuits. Figure 7 and Fig. 8 use the same notation for terminals A and B, and transistors MPO2 and MPO3. The difference currents Ic-2Igm and Ic-Igm in Fig. 7 flow into transistors MPO5, MNO1, MPO6 and MNO2 in Fig. 8. These currents are further amplified by the current mirror transistors MNO10 and MNO11 with diode-connected PMOS transistors and positive feedback transistors in the loads. The most critical part of this output circuit for the low voltage operation is the path which contains transistors MPO2, MPO5 and MNO1, or transistors MPO3, MPO6 and MNO2. In case we need the voltage Δ for keeping transistors operate in saturation region, the minimum supply voltage VDDmino for the output circuit becomes;

$$VDDmino=Vth+3\Delta \quad (2)$$

When Vth=0.2V and Δ=0.25V, VDDmino is 0.95V. The designed circuit has the very low voltage operational capability.

4. Simulation results

The performance of the VCO circuit has been estimated by the SPICE circuit simulation. Device parameters of 0.6μm transistors have been assumed. Threshold voltages (Vth) are 0.2V and -0.2V for a NMOS transistor and for a PMOS transistor, respectively. Figure 9 is the VCO oscillation frequency v.s. control voltage characteristic. Supply voltage VDD is 1V. The VCO oscillation frequency ranges from 200MHz to more than 1.4GHz. A linear relationship is also observed. Figure 10 shows the waveforms of I/Q outputs. VDD is again 1V, and the oscillation frequency is 1GHz. Phase difference of $\pi/2$, and 350 μAp-p of output current are observed. The output current is large enough to drive other circuits. In actual LSI implementation, Vth variation of transistors always occurs. Therefore, we need to check the influence. Figure 11 shows phase errors between I and Q outputs, which is the deviation from $\pi/2$. This simulation is carried out with changing Vths of all the transistors in Q-channel while Vths of all the transistors in I-channel remain unchanged. Each channel consists of three gm cells and an output circuit. The influence for the gm cell is small, however, the phase error in output circuit reaches more than 7 degree when Vth changes 10mV. This is because the current in the output circuit also changes as Vth changes and the current from gm cells changes. The current in the output circuit can be adjusted by changing the constant current source IB1 in Fig. 8. With this adjustment, the phase error is suppressed to less than 1 degree. Thus, the circuit can provide the phase adjustment capability. Table 1 summarizes the performance of the designed VCO circuit. Low power dissipation of 5.7mW has been achieved.

5. Conclusion

It is concluded that the designed CMOS VCO realizes 1V and 1GHz operation while providing I/Q outputs. Low-voltage and high-frequency MOS analog function can be achieved for the future system-on-a-chip LSIs. Noise and jitter problems should be investigated. It is also necessary to verify the circuit performance with the actual IC chip fabricated. These are remaining items for future studies.

References

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[2] K.Yamamoto, K.Maemura, N.Andoh and Y.Mitsui, "A 1.9-GHz-Band GaAs Direct-Quadrature Modulator IC with a Phase Shifter", IEEE J.Solid State Circuits, Vol.28, No.10, pp.994-1000, October 1993.

[3] B.Razavi and J.J.Sung, "A 6 GHz 60 mW BiCMOS Phase Locked Loop", IEEE J.Solid State Circuits, Vol.29, No.12, pp.1560-1565, November 1994.

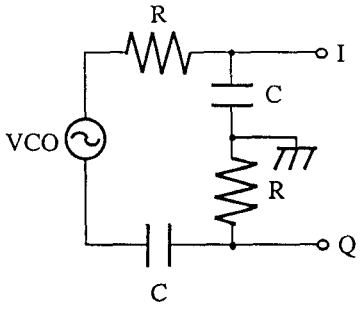

Fig. 1 Conventional RC phase shifter circuit

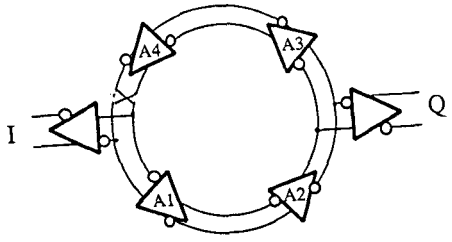

Fig. 2 Generation of I/Q outputs in a ring-oscillator type VCO

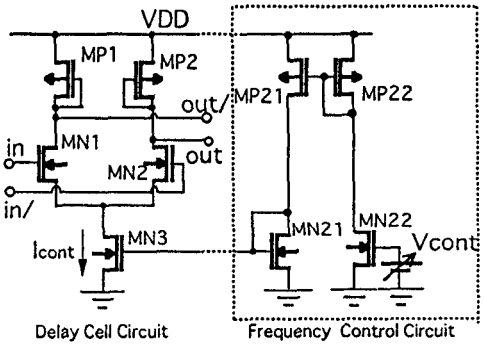

Fig. 6 The delay cell and control circuits

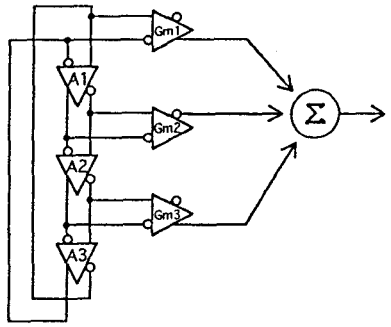

Fig. 3 The configuration that enables high-frequency oscillation

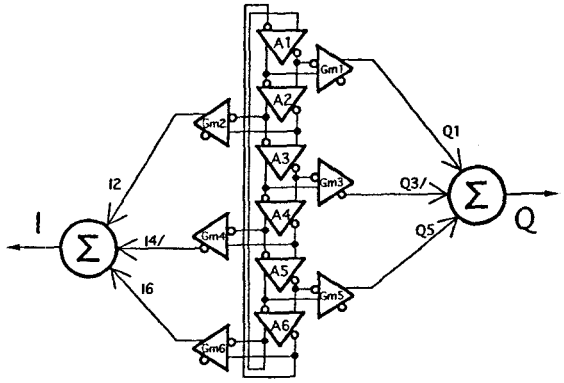

Fig. 4 The new configuration that realizes both high-frequency oscillation and generation of I/Q outputs

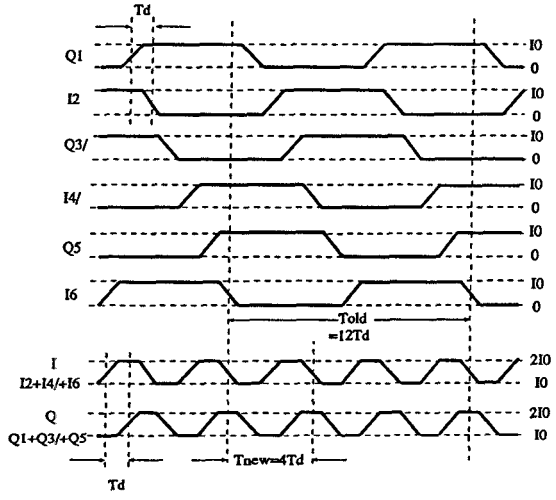

Fig. 5 Waveforms of the circuit in Fig. 4 at different places

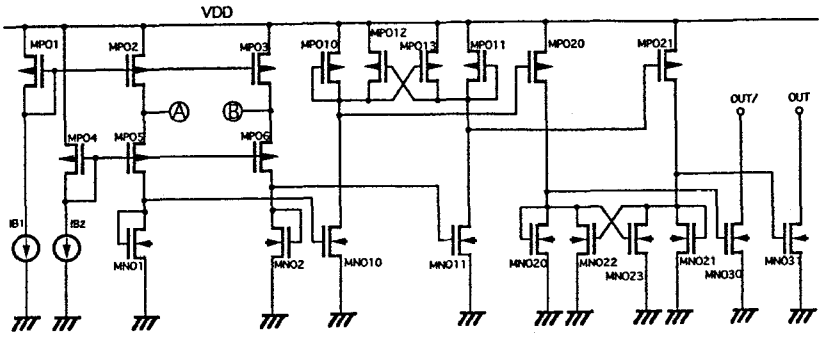

Fig. 8 The output circuit

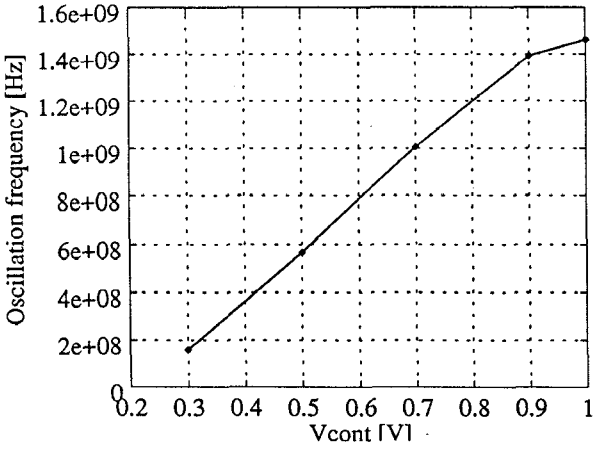

Fig. 9 VCO oscillasion frequency versus control voltage characteristic

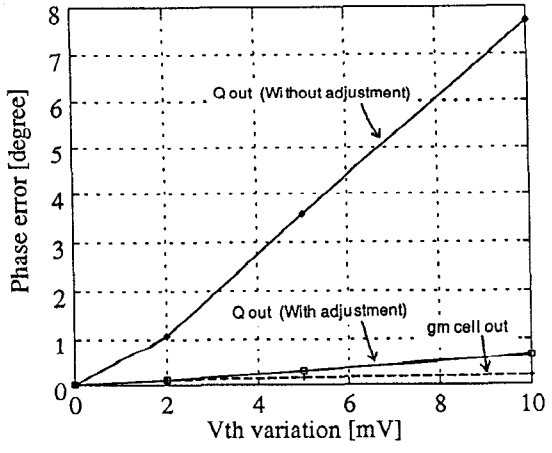

Fig. 11 Phase error at Q output with Vth variation relative to I output

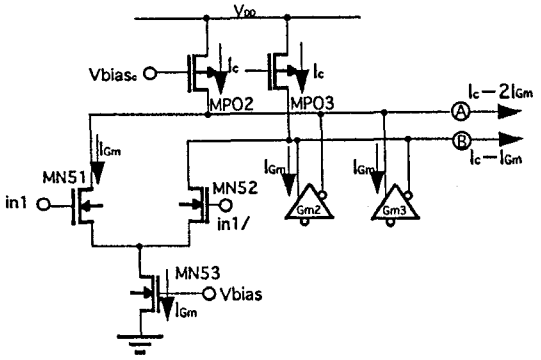

Fig. 7 The gm cell circuit and a current composing scheme

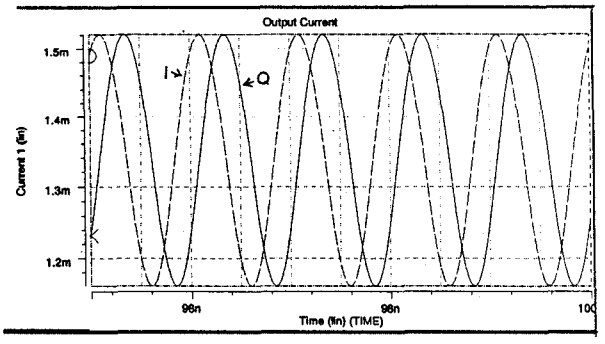

Fig. 10 Waveforms of I and Q outputs

Table 1 Overall performance of the designed VCO circuit

Items	Value	Unit
Supply voltage	1	V
Oscillation frequency range (VDD=1V)	200~1400	MHz
Power dissipation (Vcont=0.65V)	5.7	mW
Threshold voltage PMOS NMOS	-0.2 +0.2	V
Process	0.6μ CMOS	