A 1.6V 10-bit 20MHz Current-mode Sample and Hold Circuit

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Abstract

A current mode sample and hold circuit has been designed to examine if high-precision current processing is possible simultaneously with a circuit to which current mode and switched-current circuits are applied and which operates at high-speed and with low supply voltage. The results are 10-bit accuracy, a 20MHz clock, and a 2V supply voltage. Clock feedthrough which degrades the precision of current when it is processed in a switched-current circuit is effectively canceled by the use of the newly developed differential configuration.

1. Introduction

Today, analog circuits must operate with supply voltages below 3V because battery operated personal and mobile equipment is increasing rapidly. High-frequency operation and high-quality analog signal processing are still needed even with lower supply voltages. Reducing the supply voltage while maintaining high speed and precision is a major challenge for analog circuits. Signal voltage instead of signal current has usually been processed in analog circuits. The lower the supply voltage, the smaller the dynamic range becomes. This makes signal voltage processing difficult. As a result, the use of current mode and switched-current circuits has been studied intensively.[1] These circuits process a signal current which is applied to a low impedance node and produce only a small voltage swing at each node. This enables circuits operate at low voltages, high-frequency and/or high speed.[2] However, in general, it is extremely difficult to maintain precision in processing current, resulting in poor analog performance. One reason precise current processing is not possible is the poor transistor output resistance. Another is the clock feedthrough of a MOS switch which is used in a switched-current circuit.[3] Therefore, switch feedthrough suppression and output resistance increase are urgently required to achieve precision. The purpose of this paper is to examine if switch feedthrough can be canceled and if output resistance can be increased effectively while operating circuits at high speed and with low voltage. To investigate these points, a video-speed sample and hold circuit was designed. The details are described below.

2. Feedthrough Cancellation

Precise matching of input and output currents in a circuit is required to achieve high-precision analog operation. A basic current memory cell which is used in a switched-current circuit is shown in figure1.[1] It memorizes the input current Iin plus a constant current J when switches SW1 and SW2 are on in the $\phi 1$ phase. Cg is the gate-to-source capacitance of M1. As the capacitor Cg memorizes the voltage, the same amount of current of Iin plus J flows in M1 when switches SW1 and SW2 become open and SW3 connects to an output terminal in $\phi 2$ phase. However, the output current does not become equal to the input current due to clock feedthrough from switch SW1 and due to the voltage change at the output terminal. We assume, for the moment, that the voltage change at the output terminal is somehow suppressed to a satisfied level. In order to eliminate the clock feedthrough error, a differential type configuration shown in figure2 has been developed.[1] M1 and M2 form a differential amplifier with switches SW1-1 and SW1-2 at each gate. Differential input currents Iin and Iin/ are supplied to M1 and M2 via switches SW2-1 and SW2-2 in $\phi 1$ phase. Differential output currents Iout and Iout/ flow via switches SW3-1 and SW3-2 in $\phi 2$ phase. Clock feedthrough is canceled by the common mode rejection characteristic of the differential amplifier. However, this circuit needs differential inputs and outputs and six switches to operate, resulting in a very complicated circuit. It also requires precise switch timing. Thus, a simpler way of canceling clock feedthrough is necessary.

We utilized the circuit shown in figure3 as a basic current memory cell because it requires only one switch.[1] M1 and M2 form the usual current mirror. Iin

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and a constant current J always flow in M1, and Iout equals to the input current due to the current mirror action of M1 and M2 when SW1 is on in $\phi 1$ phase. An appropriate charge is stored in the gate-to-source capacitance Cg of M2. When SW1 becomes off, M2 pulls down the current which is Iin plus J at the time of switch off because Cg memorizes the voltage. Differential type configuration of the circuit in figure3 is shown in figure4. M1 and M2 together with a constant current source 2Is form a differential voltage-to-current converter with switches SW1-1 and SW1-2 at each gate. M5, M7, 2Ie, M9 and M10 form a buffer amplifier whose voltage gain is one. Without Iin, the voltage at terminal IN becomes equal to the bias voltage VB. When Iin is applied to terminal IN, Ie plus Iin/2 flows in M5 and Ie minus Iin/2 flows in M7, producing the voltage difference ΔVi. We assume the size of M1, M2, M5 and M7 are identical. ΔVi becomes,[4],[5]

$$\Delta V_{in} = V_{gs1} - V_{gs2} = \sqrt{\frac{1}{\beta_n}} \cdot \left(\sqrt{2I_e + I_{in}} - \sqrt{2I_e - I_{in}} \right) \quad (1)$$

where $\beta = \mu nCox(W5/L5)$

When switches SW1-1 and SW1-2 are on, this ΔVi is applied to the inputs of a differential voltage-to-current converter and is converted to I1 and I2. If we take I1-I2 as the output current Iout, then ,

$$I_{out} = \beta \sqrt{\frac{2I_s \Delta V_{in}^2}{\beta} - \frac{\Delta V_{in}^4}{4}} = I_{in} \sqrt{1 + \frac{4}{I_{in}^2}(I_s - I_e)\left\{2I_e - \sqrt{(2I_e)^2 - I_{in}^2}\right\}} \quad (2)$$

When Ie=Is is selected, the second term in the root in equation (2) becomes zero and,

$$Iout = Iin \quad (3)$$

is obtained. When the switches turned off, ΔVi is stored in gate-to-source capacitors M1 and M2, enabling Iout to equal that in equation(3). Clock feedthrough from switches is eventually suppressed by the common mode rejection characteristic of the differential voltage-to-current converter. The desired sample and hold action of input current is performed.

3. Increasing transistor output impedance

Another problem that must be solved is the error which occurs when drain-to-source voltages of transistors differ. In figure3, for example, output current Iout differs from Iin plus J if the voltage at the output terminal, that is, the drain-to-source voltage of M2 differs from the drain-to-source voltage of M1. Even when the voltage at the output terminal is biased equal to the drain-to-source voltage of M1 in DC conditions, the drain-to-source voltage between M1 and M2 differs when an AC input current is applied. This is caused by the inverting action of the input signal of the circuit and produces an error in current ratio which is dependent on the input signal. To avoid this, each mirror transistor should have a cascode transistor. The resulting circuit is like the one shown in figure5. M3 and M4 are cascode transistors for M1 and M2. The Vbias voltage should be chosen so as not to drive M1 and M2 into saturation. The voltage change at drain terminals of M1 and M2 can be minimized, as can the output current variations with input signal.

4. Sample and hold circuit

The whole schematic of a sample and hold circuit is shown in figure6. For switches SW1-1 and SW1-2, the combination of an NMOS transistor and a PMOS transistor is used. These are controlled by the 20MHz clock applied to the gate of switching transistors. The output circuit, which consists of transistors M11 to M18, obtains the difference of currents I1 and I2. It is a typical folded cascode circuit, and Iout becomes I1-I2. Cascode transistors M3, M4, M6, M8, M16 and M18 are used to prevent mirror transistors M1, M2, M5, M7, M15 and M17 from being affected by input signals. Although clock feedthrough from switches is effectively canceled by adopting the differential configuration, it is still not canceled enough to achieve 10-bit accuracy as a sample and hold output. To further suppress clock feedthrough from switches, 0.3pF capacitors Cgd1 and Cgd2 are connected to gates of M1 and M2. We must be careful not to make the capacitors to large because the on resistance of the switch and capacitor determines the high-frequency characteristics of the circuit. Constant currents Ib1 and Ib2 shift the level at the node to which the drain of M8 and the drain and a gate of M9 are connected. The voltage at this node becomes equal to that of the terminal IN when Iin is not applied. When Iin is applied, M9 and M10 are selected such that the voltage change at this node tracks the voltage at the terminal IN.

5. Simulation Results

We simulated the performance of the circuit in figure6 using the SPICE circuit simulation program. First, we examined circuit performance with a power supply of 3V. Device parameters of transistors are consistent with the 1.2 μm design rule. Threshold voltages (Vth) are 0.92V for an NMOS transistor and -0.85V for a PMOS transistor. Input current is $\pm$20 μA triangular waveform. 2Is and 2Ie are chosen to be 200 μA. The clock rate is 20MHz and power dissipation is 2.4mW. Figure7 shows the waveforms of input current and output current when the input current frequency is 1MHz. One step of hold current becomes 4.0 μA. The deviation from the step is observed to be $\pm$0.003 μA. This corresponds to less than 0.01% of linearity. Acquisition time to 0.1%

is 16ns, and -3dB bandwidth of the circuit is 90MHz when switches are on. Performance is adequate for a 10-bit 20MHz sample and hold circuit. The gain error, which is the total difference between input and output current when switches are all on, is also measured as shown in figure8. When input frequency increases, the error increases. It turns out that the error depends on the size of switch transistors and disappears when switches are replaced by pure resistors of 2.3kΩ. One reason is that it is due to the on resistance modulation of switches by an input signal. The solution of this problem is left for further research.

The circuit in figure6 is also simulated by using device parameters of the 0.6 μm design rule. Threshold voltages is 0.4V for an NMOS transistor and -0.4V for a PMOS transistor. Input current is ±20 μA, 2Ie and 2Is become 100 μA, and supply voltage is 1.6V. Clock frequency 20MHz does not change. Device sizes are changed to suit for this 1.6V operation. Waveforms with 1MHz and 5MHz input frequencies are shown in figure9(a) and figure9(b). The linearity becomes 0.025% for the 1MHz input and 0.1% for the 5MHz input. The -3dB bandwidth is 90MHz and acquisition time is 18ns. Power dissipation is 1.2mW. The circuit performance and circuit and device parameters are listed in table1.

6. Conclusion

The circuit in figure6 achieves 10-bit 20MHz sample and hold operation with supply voltages of 3V and 1.6V. Reduction of supply voltage depends strongly on the threshold voltage of transistors. However, application of current mode and switched-current circuits is becoming very useful for realizing low-voltage analog functions. In order to obtain high-precision characteristics, new methods to cancel the clock feedthrough and to increase the output resistance of a device are developed and applied. These new methods make possible realization of high-precision, high-speed and low-voltage operation simultaneously with current mode and switched-current circuits. Even more applications of current mode and switched-current circuits to other analog functions in low voltage operation area are desired.

References

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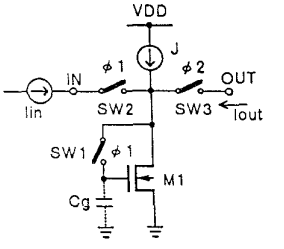


Fig. 1 Basic current memory cell No.1

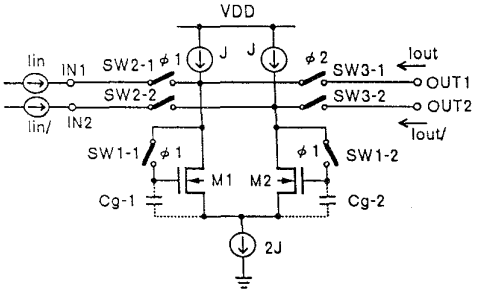


Fig. 2 Differential current memory cell

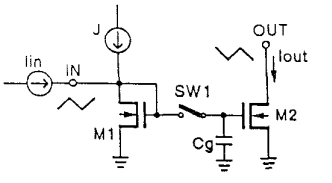


Fig. 3 Basic current memory cell No.2

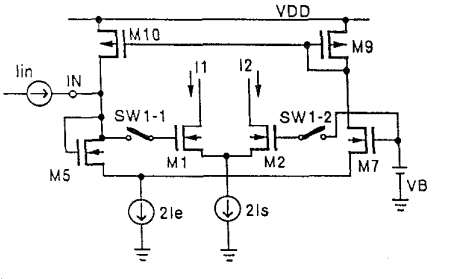


Fig. 4 New differential current memory cell

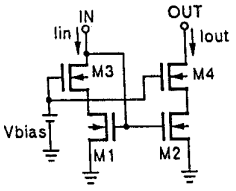


Fig. 5 Current mirror with increased output impedance

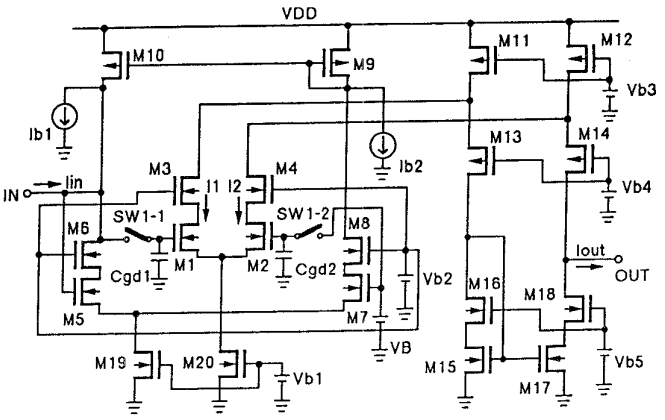


Fig. 6 Sample and hold circuit

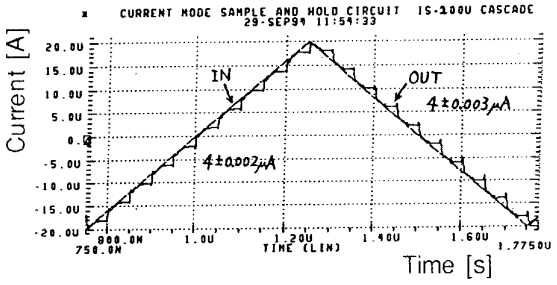
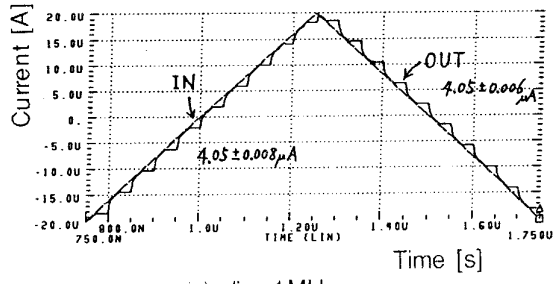
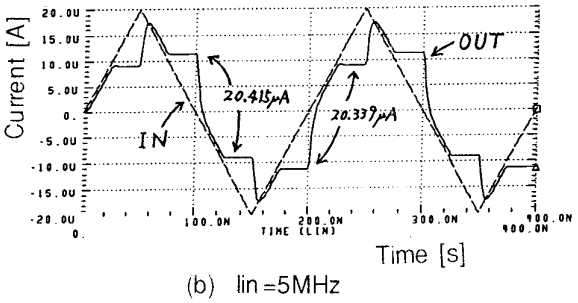


Fig. 7 Input and output current waveforms (Vdd=3V, Iin=1MHz, Clock=20MHz)



(a) Iin=1MHz



(b) Iin=5MHz

Fig. 9 Input and output current waveforms (Vdd=1.6V, Clock=20MHz)

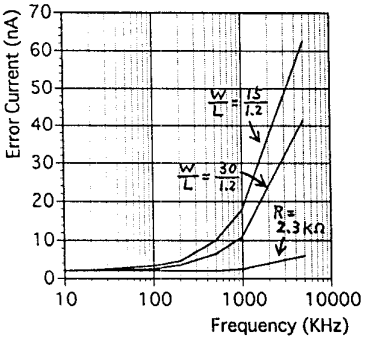


Fig. 8 Gain error

Items	VDD=3V	VDD=1.6V
Threshold voltage NMOS	+0.92V	+0.4V
Threshold voltage PMOS	-0.85V	-0.4V
Input current	±20 μA	±20 μA
Bias current 2Ie	200 μA	100 μA
Bias current 2Is	200 μA	100 μA
Sampling frequency	20MHz	20MHz
-3dB bandwidth	90MHz	90MHz
Capacitor value Cgd1=Cgd2	0.3pF	0.3pF
Linearity	less than 0.01%(1M)	0.025%(1M) 0.1% (5M)
Acquisition time (0.1%)	16ns	18ns
Power supply	3V	1.6V
Power dissipation	3mW	1.2mW

Table1 Overall performance of the circuit in figure6