

A VARIABLE DELAY GENERATOR for DESKEW IC
using ECL GATE ARRAY

S.Nitta, T.Sugoh, H.Sugiyama, M.Nakamura, Y.Sugimoto, Y.Fukai,
K.Hirakawa, H.Takada, S.Sakoh, H.Sawaya, T.Fujita, T.Miyazaki
and N.Itoh

Toshiba Corporation

580-1, Horikawa-cho, Saiwai-ku,
Kawasaki 210, Japan

1. Introduction

Recent progress in LSI testers requires high speed and high performance deskew ICs to eliminate the timing difference between signals. The one chip realization of the deskew function is also inevitable to realize the instrument to be much more compact. The coexistence of analog and digital functions, and the need to use ECL logics, however, have prevented it to be integrated on a conventional ASIC chip. We have newly developed the deskew IC with all the necessary functions on a 3K gate ECL gate array adopting differential logic scheme together with a new delay generator and DAC macrocells. As a result, the minimum cross talk noise within a chip and the high resolution in delay time have been realized.

2. Variable Delay Generator

The Variable Delay Generator (VDG) is a main function in a deskew IC. The control of a signal delay time in high resolution is necessary. FIG.1 shows the block diagram of a VDG. It contains one variable delay, four fixed delays, a 6bit DAC, and a 5 to 1 multiplexer. The delay time of the variable delay, which is controlled by the output voltage of the 6bit DAC, ranges from 0 to 1.8ns. Both rising and falling edges can be delayed equally. This enables a minimum pulse width in a delay block to be 3ns. The delay time of fixed delays is set to 1.6ns. Five delay blocks are connected in series and the total adds up to 8.2 ns. As the DAC has 6bit resolution, the minimum step in delay time becomes 29ps. Arbitrary delay time within 8.2ns can be realized selecting one output out of five delay blocks in the 5 to 1 multiplexer which is controlled by 16 \times 18 in FIG.1. The VDG utilizes ECL logics with a fully differential architecture to minimize cross talks and to increase the noise immunity. The VDG has been realized on an ECL gate array chip using the Advanced Silicon bipolar Technology II (AST-II) process with features of double-polysilicon, self-aligned emitter-base structure and trench isolation. A NPN transistor has the minimum emitter size of 0.5 μ m and cut-off frequency of 15GHZ.

3. The New Delay Line Configuration

The newly developed delay line macrocell has features of varying capability of both rising and falling edges and low noise capability. FIG.2 and FIG.3 show the detail of the variable delay appeared in FIG.1. There are two ramp generators and comparators in FIG.2. The first ramp generator produces a ramp waveform only for the falling edge of the incoming signal. The first comparator compares the DC level of this with that of the REF which is the output of a 6bit DAC and produces a pulse whose pulse width is wider than a previous one. This pulse is inverted by LSINV before applying to the RAMPGEN. With this inverted

pulse as an input, the second ramp generator produces the ramp waveform as shown in FIG.3. Although the ramp waveform generation at the second RAMPGEN is now performed for the falling edge of the LSINV output, this is equivalent to the ramp waveform generation for the rising edge of the original input signal to the variable delay. The second comparator compares the DC level of the second ramp generator output with that of REF and produces the resultant delayed pulse with the same pulse width as an input. This delayed pulse generation scheme is very much fit for handling the signal with narrow pulse width because there does not exist any intermediate pulse with its pulse width narrower than an input. All the input and output of each block except for the output of RAMPGENs consist of differential signals in FIG.2, which enables the variable delay have a large noise immunity and less cross talk generation. The circuit of the RAMPGEN macrocell is shown in FIG.4. There appears 15 transistors at the output Z. These transistors are used as a loading capacitor instead of using an actual capacitor because the base array of a 3K gate ECL gate array does not contain any capacitor in it. The ramp generation is performed by pulling out charges stored in this equivalent capacitor using the constant current source. The ramp waveform is only obtained for the falling edge of the signal at Z. Due to the large driving capability of an emitter follower, the voltage at Z rises quickly. The operation of delay generation in fixed delays is exactly the same as that of the variable delay. Time delay is fixed to be 1.6ns by applying the fixed voltage to REF terminal.

4. DAC Circuit

A 6bit DAC has also been implemented on the base array. The difficulty does exist in usual to implement a DAC on the conventional gate array because the output DC level should be matched to that of the ramp generator in FIG.4. The circuit of a 6bit DAC is shown in FIG.5. The DAC consists of the combination of segmented current sources and R-2R ladder network. The output swing is nearly equal to $2I_0 R_0$, where I_0 is the current of one differential pair in FIG.5. The same current source as one used in the ramp generator in FIG.4 is also used in configuring this DAC circuit in FIG.5. When we chose R_0 in FIG.5 to be half value of RC in FIG.4, the voltage swing of the DAC becomes almost the half of that of the ramp generator. This guarantees the inclusion of the DAC voltage swing in the range of the ramp generator voltage swing. The initial DC level of the DAC can be set using resistors and transistors connected in the manner shown in FIG.5. In this way, the DAC with matched output voltage and swing level is implemented on the base array of an ECL gate array.

5. Results

Integrating 12 variable generators and logics on a 3K gate ECL gate array, a deskew IC is realized. FIG.6 is the measured delay of the variable delay block in FIG.1. The fixed delay is introduced by I/O buffers, a multiplexer and so on. Almost 1.8ns of variable delay is obtained by changing steps of the DAC. This shows that the delay line implementation on a gate array is effective for realizing a deskew IC.

6. Summary

The deskew IC with 12 newly developed VDGs has been implemented on a single 3K gate gate array chip. The use of a fully differential architecture and ECL logics enables the cross talk noise minimum. The newly developed VDG has the resolution of time delay of 29ps and the variable time delay capability up to 8.2ns. It is also confirmed that the one chip realization of the deskew function greatly saves the packing space of an instrument.

7. Reference

[1] Y.Kamimoto et al., "Bipolar Monolithic Programmable Delay Generator," Paper of Integrated Circuits Study Group, IEICE, ICD90-47, pp23-30, 1990.

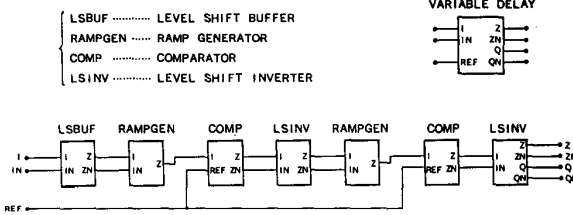


FIG. 2 Variable Delay Block Diagram

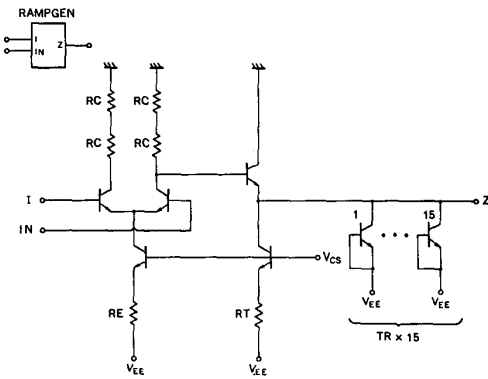


FIG. 4 Ramp Generator Circuit

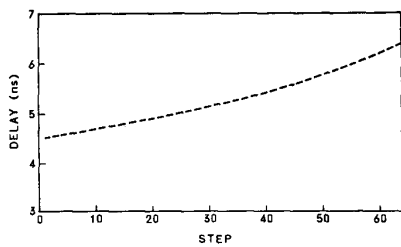


FIG. 6 Delay vs DAC Control Bit Step

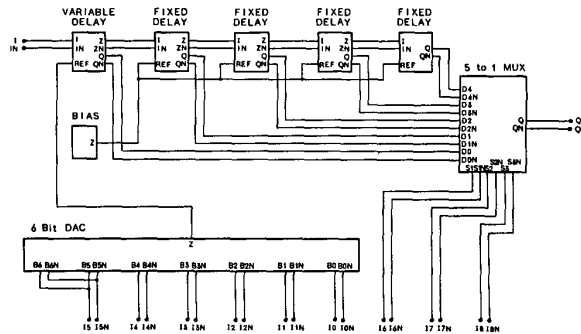


FIG. 1 Block Diagram of a Variable Delay Generator

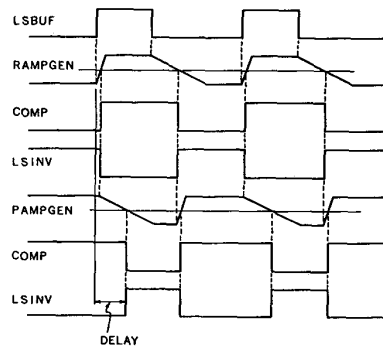


FIG. 5 Output Waveforms of Variable Delay Block

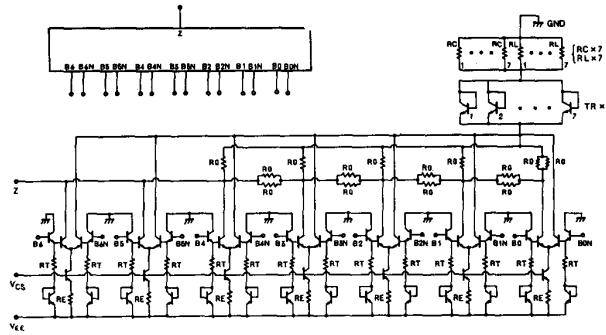


FIG. 5 6 Bit DAC Circuit

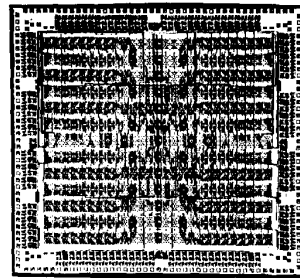


FIG. 7 Chip Photomicrograph