A 10BIT 40MHz ADC USING 0.8um BI-CMOS TECHNOLOGY

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ABSTRACT

A 10bit ADC has been developed using 0.8um Bi-CMOS technology. In order to reduce power dissipation and chip size, two-step parallel type conversion scheme is adopted. 10bit resolution has been realized at the maximum conversion rate of 40MHz, power dissipation of 700mW and chip size of 4.1x4.8mm^2.

INTRODUCTION

The expectation of low power and low cost monolithic 10bit ADC is growing for application to digital video equipments and high diffinition TV. Fully parallel type 10bit video ADCs have already been fabricated in bipolar process [1,2]. However, they require large power dissipation, chip size and big package. Two-step parallel type conversion architecture has decreased power and chip size by 1/2 to 1/3 of those of fully parallel type ADC [3]. But it still consumes power and chip area. CMOS technology is able to decrease them more and more. However, it is difficult to realize both 10bit resolution and video speed by utilizing CMOS process.

Therefore, we have proposed use of Bi-CMOS circuits and process technology, because high speed and high resolution bipolar comparator, ideal analog switch and low power CMOS logic can be used. We have fabricated 10bit video ADC using 3um Bi-CMOS process and obtained the maximum conversion rate of 10MHz [4]. But, it is not enough for application to digital video equipments. This paper discribes a 10bit two-step parallel type ADC with small power dissipation and chip size fabricated in 0.8um Bi-CMOS process. It has the maximum conversion rate of 40MHz being applicable to digital video equipments.

CIRCUIT CONFIGURATION

In two-step parallel conversion scheme, the method to link each bit in coarse and fine ADC is most important. It is difficult to obtain 10bit resolution for a conventional two-step parallel type ADC using a DAC and a subtractor because of inconsistent between gain of the subtractor and full scale range of fine ADC. Also, small settling time is required for the subtractor.

Here, we adopt the scheme transforming coarse reference voltages to fine ladder resistors using buffer amplifiers. As emitter follwer circuit can be used for the buffer amplifier, small settling time is obtained. Additionally, we also adopt the subranging architecture in which the full scale range of fine ADC is consistent with the equivalent voltage to 1.5LSB for coarse ADC. According to this architecture, 10bit resolution is not required for coarse ADC, and total resolution is decided by fine ADC.

Figure 1 shows the block diagram of a Bi-CMOS 10bit 40MHz ADC. This system consist of 5bit fully parallel type coarse ADC, 5.5bit fully parallel type fine ADC, analog switches, buffer amplifiers, CMOS logic circuits and output buffers. The fine ADC have additional 0.5bit to compensate the coarse ADC error, the voltage shift which may be produced in the process of voltage transformation from coarse to fine ladder resistors, or the voltage variation occured due to sample and hold output settling. Bipolar comparators with input offset voltage less than 0.5mV are used in both the coarse and fine ADC to obtain 10bit resolution in more than video speed. In the case of a CMOS comparator, equivalent input offset voltage increases as input frequency increases because loop gain decreases rapidly.

The buffer amplifier in Figure 1 is a bipolar emitter follower with V_{BE} mismatching less than 0.5mV. Therefore, the precise voltage transformation from coarse to fine ladder resistors is possible. The voltage transformation is performed by PMOS analog

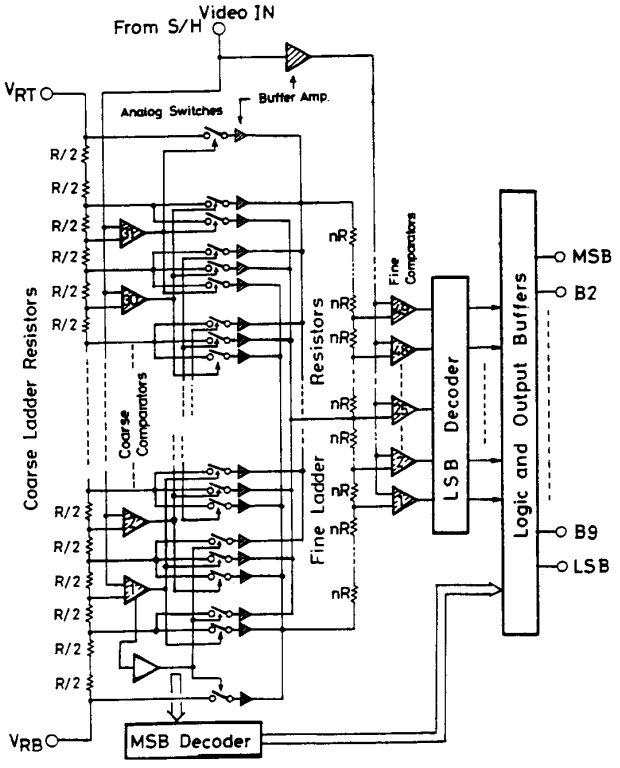

Fig.1 Block Diagram of a 0.8um Bi-CMOS 10bit ADC

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switches prepared in coarse ladder network. The analog switches are controlled by outputs of coarse latching comparators. So as to perform the correction in the fine ADC, two LSB equivalent voltage of the coarse ADC is transformed. The settling time of fine ladder resistors is about 10ns.

Logic and output stage in Figure 1 is composed of CMOS and Bi-CMOS logic circuits to reduce power and chip size.

The shaded portions in Figure 1 are the places where bipolar analog circuits are used.

SUBRANGING ARCHITECTURE

We explain the subranging architecture in the ADC using Figure 2. Input signal 1 is input to the coarse ADC and a input buffer for the fine ADC. At the first, the input signal 1 quantized by sample and hold circuit is converted to 5bit data by the coarse ADC. We call them "Temporal MSB Data". At the same time, three analog switches selected by the coarse comparator outputs turn on, and two LSB equivalent voltage of the coarse ADC is transformed. After that, the output of the fine ADC input buffer (input signal 2) is converted to 5bit data by the fine ADC.

The conversion by the fine ADC is performed under the full scale range of 1.5LSB extended by 0.25LSB at the both sides of range corresponding to the "Temporal MSB Data". Therefore, 10bit resolution is not required for the coarse ADC.

If the fine A/D conversion is performed in the extended range, signals to correct the "Temporal MSB Data" are output from the fine ADC. They are shown by "+1" and "-1". The "Temporal MSB Data" are added or subtracted 1bit by these signals. After the correction, final MSB data are decided.

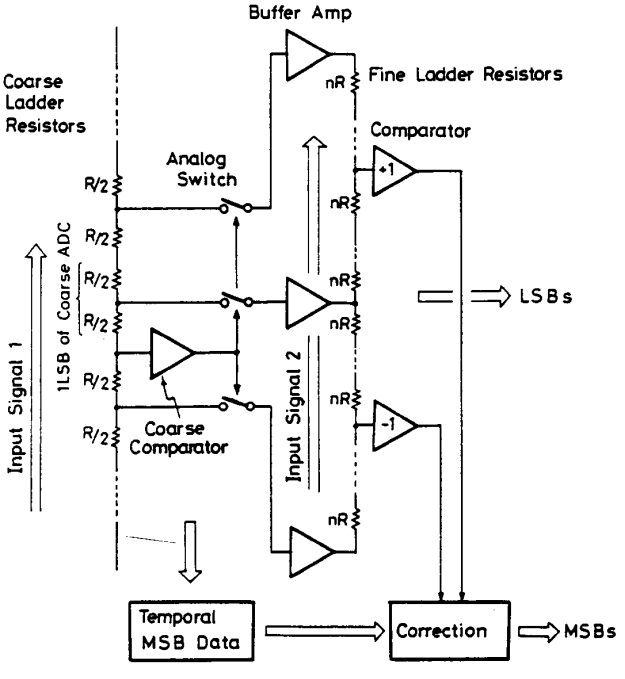

Fig.2 Subranging Architecture

BI-CMOS CIRCUIT DESIGN

Figure 3 shows the coarse latching comparator circuit which consists of a bipolar amplifier stage and a CMOS latch stage. The reasons for using the CMOS latch circuit are to reduce the time required for conversion of small voltage swing from the amplifier stage to CMOS level swing, and to reduce power and chip size. To use the CMOS latch circuit, gain of the bipolar amplifier stage is 39dB which is larger than that of conventional bipolar comparator. The CMOS latch circuit is of form of inverter flip-flop for high speed. M1 to M4 in Figure 2 are analog switches separating the latch circuit from the amplifier stage at holding mode. To reduce the influence of clock feedthrough, CMOS switches are used. M5 and M10 are the switches to latch the inverter flip-flop composed of M6 to M9.

As described before, total ADC resolution is determined by fine latching comparators. For this reason, they are composed of bipolar differential amplifiers. For simplicity and speed-up, decoder logic for fine ADC is also composed of the bipolar wired OR logic. The small voltage swing output from the wired OR ($600mV_{p\text{-}p}$) is converted to CMOS level swing by bipolar differential amplifier and MOS current mirror circuits. The bipolar wired OR and the level conversion circuits are shown in Figure 4. The propagation delay time of the level conversion circuit is about 3ns.

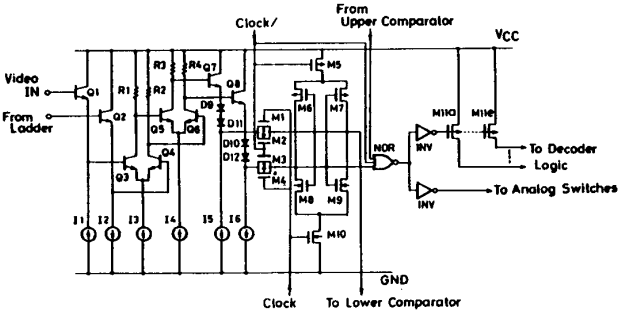

Fig.3 Coarse Comparator Circuit

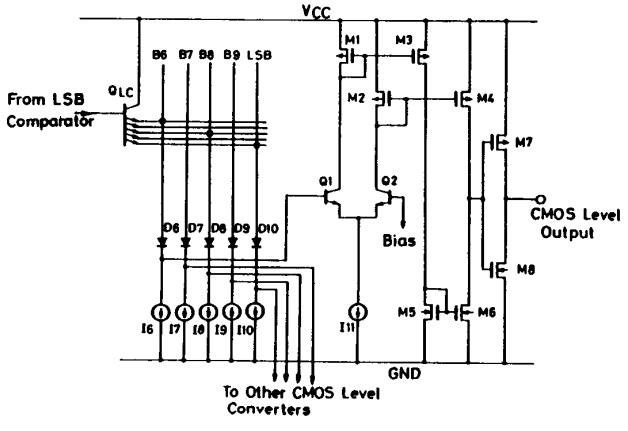

Fig.4 LSB Decoders and An ECL to CMOS Level Converter

Figure 5 shows the analog switch and the buffer amplifier which transform the reference voltage from coarse to fine ladder network. The deviation of voltage drop by M1 and V_{BE} mismatching of Q1 must be below 10bit resolution. The dimension of M1 is decided considering the deviations of threshold voltage, channel length and base current of Q1. ON-resistance of M1 is 200 ohm. V_{BE} mismatching of Q1 is below 0.5mV. M2 is a switch to cut off Q1 completely. M1 and M2 is controlled by coarse comparator output.

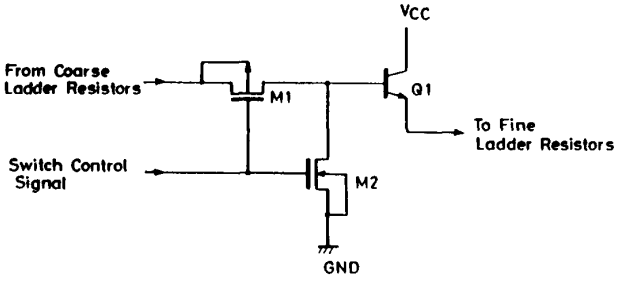

Fig.5 Analog Switch and Buffer Circuit

EXPERIMENTAL RESULTS

This LSI is fabricated in 0.8um Bi-CMOS process. An NPN transistor has ion-implanted emitter with stripe length of 2.4um and offset voltage of 0.4mV(3σ) at S_e=8x8um^2. f_{TMAX} is 9GHz. Channel length of an NMOS transistor is 0.8um, and that of a PMOS transistor is 1.0um. Poly-Si resistor and L-PNP can be used. Ladder network is composed of $MoSi_2$ resistors so that reliability of the chip can be enhanced. The mismatching of $MoSi_2$ resistors is 0.1% on one chip.

Figure 6 is a photograph of the reconstructed triangular waveform and the linearity error at 40MHz sampling rate. Input frequency is 10kHz. The error falls within 2mV. Figure 7 shows a beat sine waveform for 10.01MHz sampling rate and 10MHz input frequency. Input bandwidth is above 10MHz. The characteristics for the differential gain and differential phase are shown in Figure 8 (a) and (b), respectively. The differential gain is 0.5% and the differential phase is 0.7degree at 14.3MHz sampling rate. The chip performance is summarized in Table 1. Static power dissipation and chip size are 700mW and 4.1x4.8mm^2 for 10bit resolution. Total elements count is 7000. Bipolar transistor takes about 3000, MOS transistor takes about 3000, and resistor takes about 1000. The ADC can operate with 5V single power supply. Figure 9 shows a microphotograph of the 10bit ADC.

CONCLUSION

The 10bit 40MHz ADC has been developed by utilizing Bi-CMOS circuit and 0.8um process technology. Bipolar amplifiers and comparators have realized 10bit resulution and 40MHz operation. Two-step parallel type conversion scheme, MOS analog switches and CMOS logics have realized chip size of 4.1x4.8mm^2 and power dissipation of 700mW.

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References

[1] T.Takemoto, M.Inoue, H.Sadamatsu, A.Matsuzawa and K.Tsuji, "A Fully Parallel 10-Bit A/D Converter with video speed," IEEE Journal of Solid-State Circuits,Vol.SC-17, No.6, pp.1133-1138, December 1982.

[2] "Single-chip 10-bit flash ADC samples at a 50-MHz rate," Electronic Design, pp.49-52, September 3, 1987.

[3] T.Shimizu, M.Hotta and K.Maio, "A 10-bit 20MHz Two-Step Parallel A/D Converter with Internal S/H," IEEE Journal of Solid-State Circuits, Vol.24, No1, pp.13-20, February 1989.

[4] Y.Sugimoto and S.Mizoguchi, "AN EXPERIMENTAL BI-CMOS VIDEO 10BIT ADC," Proceedings of the 1988 Symposium on VLSI Circuits, pp.129-130, August 1988.

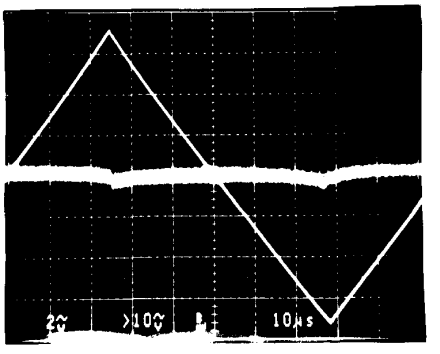


Fig.6 Reconstructed Triangular Waveform and Linearity Error at 40MHz Sampling Rate.
Reconstructed Waveform ; 1Vp-p,10kHz.
Linearity Error ; 20mV/div.

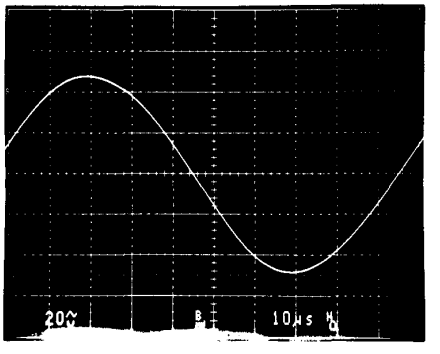
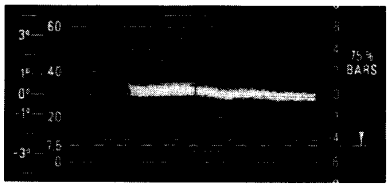
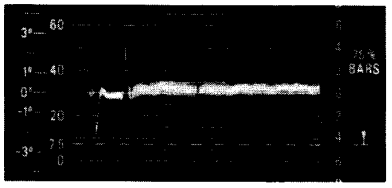


Fig.7 Beat Sine Waveform for 10.01MHz Sampling Rate and 10MHz Input Frequency.
Vertical ; 200mV/div. , Horizontal ; 10us/div.



(a) Differential Gain = 0.5%



(b) Differential Phase = 0.7degree

Fig.8 (a) Differential Gain and (b) Differential Phase at 14.3MHz Sampling Rate.

Table 1 Chip Performance

Resolution	10 bit
Maximum Conversion Rate	40 MHz
Analog Input Range	3 to 5V
Power Dissipation	700mW
Supply Voltage	+5V
Elements Count	7,000
Chip Size	4.1 x 4.8 mm²
Process	0.8μm Bi-CMOS Double Metal

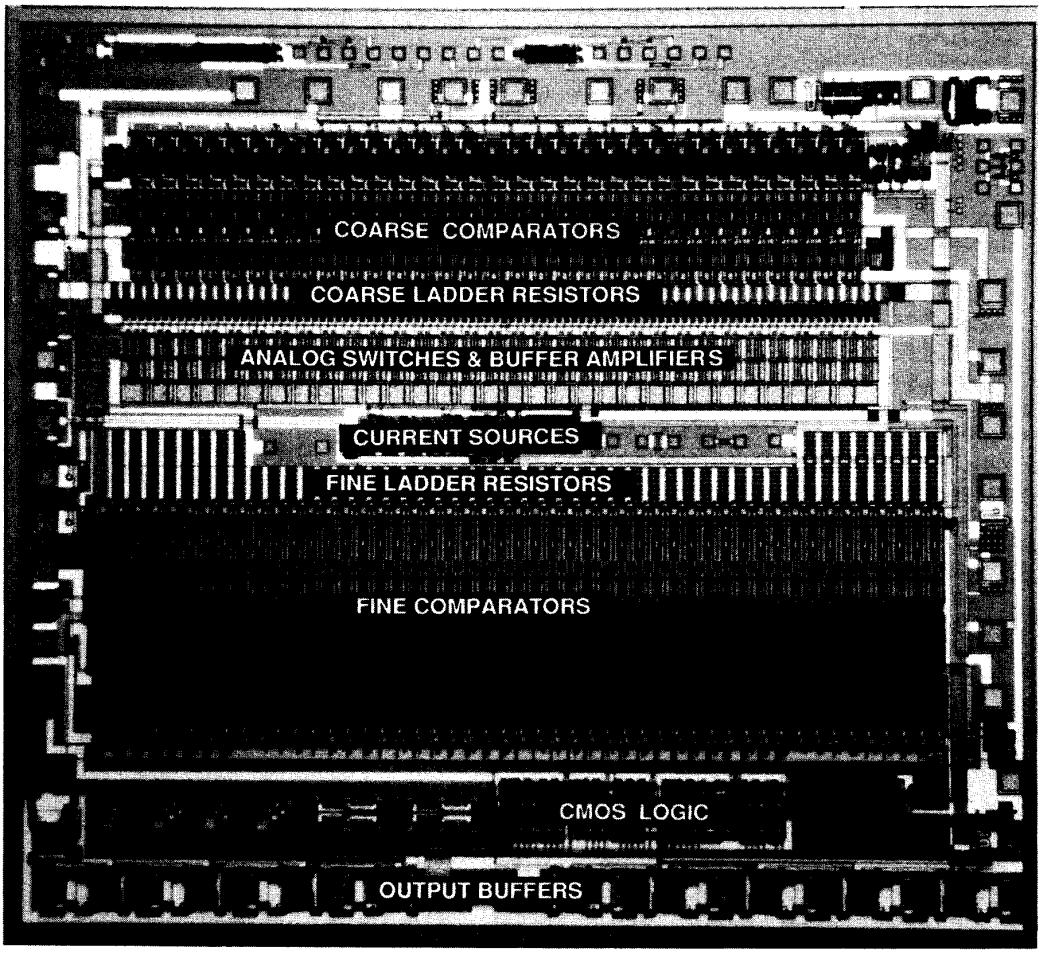


Fig.9 Microphotograph of a 0.8um Bi-CMOS 10bit ADC