A 350 ps 50K 0.8 μm BiCMOS Gate Array with Shared Bipolar Cell Structure

Hiroyuki Hara, Yasuhiro Sugimoto, Makoto Noda, Tetsu Nagamatsu,
Yoshinori Watanabe *, Hiroshi Iwai, Yoichirou Niitsu, Gen Sasaki
and Kenji Maeguchi

Semiconductor Device Engineering Laboratory, Toshiba Corporation
1, Komukai-Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan, Phone 044-549-2208
* Toshiba Microelectronics Corporation

Abstract

A BiCMOS gate array with the gate delay of 350 ps has been realized by 0.8 μm BiCMOS technology. Minimum gate delay and minimum cell area have been achieved with a shared bipolar cell structure. The gate delay is almost equivalent to that of a 0.5 μm pure CMOS gate array. Cell area increase is minimized to only 25 % compared with a 0.8 μm pure CMOS cell. I/O cells can interface with CMOS, TTL and ECL chips at the same time with a single supply voltage of 5 V.

Introduction

A BiCMOS gate array is one of the most attractive devices to realize a high performance system. However, the extra cell area for bipolar transistors requires more chip size and chip cost. Many BiCMOS gate arrays adopt a basic cell containing two bipolar transistors [1][2], and the basic cell area increases about 50 % larger than a pure CMOS cell. Recently, in order to reduce the cell area, a BiCMOS drive array with a CMOS core and peripheral BiCMOS blocks has been reported [3].

The above problem has been solved by a shared bipolar cell structure. This approach achieves a BiCMOS basic cell containing one bipolar transistor. The basic cell area becomes only 25 % larger than a pure CMOS cell, thus a high speed, high density BiCMOS gate array can be realized.

Circuit Architecture

A BiCMOS gate has an advantage over a pure CMOS gate in high loading condition. However, considering speed and cell area in low loading condition, a CMOS gate is the most suitable one. As a result of this, a BiCMOS gate is not necessarily required for every logic gate. Therefore, it is important to estimate the number of BiCMOS gates used on a chip. We have concluded that less than 50 % of BiCMOS gates out of total gates count is the best choice from the total cost performance viewpoint. Layout CAD also requires the basic cell to be uniformly laid out on a chip.

The result is a BiCMOS basic cell containing one bipolar transistor, one diffusion resistor and one pure CMOS basic cell. Basic cell area becomes only 25% larger than a pure CMOS cell. BiCMOS basic cells are arranged so that a channelless architecture can be realized. Figure 1 shows the BiCMOS basic cell pattern and the basic cell layout pattern of the BiCMOS gate array. One basic cell and one bipolar transistor of the adjacent basic cell makes one BiCMOS gate in this structure.

The structure allows us to utilize many pure CMOS macrocells and popular CMOS gate array CAD tools, and accordingly reduce the development cost. To demonstrate the usefulness of the architecture, we have designed a BiCMOS gate array with 51,012 basic cells and 188 I/O cells.

I/O Design

I/O cells consist of mixed CMOS and bipolar buffers and CMOS logic gates. These I/O cells can interface with CMOS, TTL and ECL chips at the same time with a single supply voltage of 5 V. This results in eliminating many peripheral chips that are required to interface the gate array. The delay associated with converting the level and driving the load is significantly reduced. All I/O cells are appropriately programmed by the metalization to fit the interface requirement.

The TTL output buffer in a single I/O cell can provide a sinking current of 48 mA at the TTL level. Figure 2 shows the circuit of the TTL output buffer. The buffer has the property of little ringing output in spite of large sinking current capability. This is because the bipolar transistor Q1 pulls down the output terminal first to some extent low level, and after that, 4 times larger transistor Q2 turns on to provide a large sinking current and pulls down the output close to the GND level. At this time, Q1 goes cut-off.

ECL I/O buffers can interface both with ECL 10K and

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100K levels without a negative supply voltage. Figure 3 shows the circuit of ECL I/O buffers. In the ECL input buffer, the negative voltage is applied to the emitter of the input transistor through an external resistor connected to -2 V, however, appropriate base biasing enables the input transistor to operate correctly even when there exists no negative supply on the chip. Band-gap reference generator in the ECL bias circuit provides the temperature compensated bias voltage and, as a result, the threshold voltage of -Vi-RI/2 at the input is always maintained. The ECL output buffer converts CMOS level swing into ECL level swing. The current flowing through the resistor R2 is switched by the internal signal and the resultant voltage across R2 becomes ECL level swing. The converted voltage is transferred to the output terminal with emitter followers. The output high and low voltage are -Vi and -Vi-RI, respectively. These voltages are also temperature compensated by using band-gap reference generator.

Process Technology

The chip is fabricated by using a high performance 0.8 μm double metal BiCMOS process. The process is based on the 0.8 μm CMOS process. Figure 4 shows a cross-sectional view of the 0.8 μm BiCMOS process. Only 3 extra masks are necessary to form the bipolar transistor. Buried N^+ and deep N^+ regions are necessary for collector formation, and base P^- region for base formation. P^+ contact for the base and emitter N^+ regions are formed at the same time when source and drain diffusion of MOS transistors are formed. Therefore, the cost increase can be minimized. Channel lengths for the N MOS and P MOS transistors are 0.8 μm and 1.0 μm, respectively. The emitter width of a bipolar transistor is 2.2 μm. The transit frequency (f_T) reaches to 9 GHz.

Performance

A test chip is designed to evaluate the speed of internal gates and I/Os, and to verify the yield of bipolar transistors. Figure 5 shows a microphotograph of the test chip. A BiCMOS 2-input NAND gate has achieved the delay time of 350 ps when driving the load of fanout six. Figure 6 shows the gate delay versus fanout characteristic of the BiCMOS gate compared with a pure CMOS gate.

Figure 7 shows the output waveform of the TTL output buffer. Less than 0.2 V of ringing level can be observed. Figure 8 shows the load capacitance dependency of the TTL output buffer. 3.8 ns of propagation delay in the 50 pF loading condition is realized. Figure 9 shows the waveform of the ECL output buffer. The proper conversion has been realized. The delay of the ECL output buffer is 3.9 ns in the 50 pF loading condition. Table 1 summarizes the chip performance of the 50K BiCMOS gate array. Chip size is 8.37 x 8.37 mm^2.

Conclusions

A high performance BiCMOS gate array has been developed using 0.8 μm double metal BiCMOS process. A high packing density of gates has been realized with a shared bipolar cell structure. As the BiCMOS gate is turned out to have little fanout dependency, the easy design for system people can be expected. In addition to this, ECL interface capability without a negative supply voltage is demonstrated by using BiCMOS circuit and process technology.

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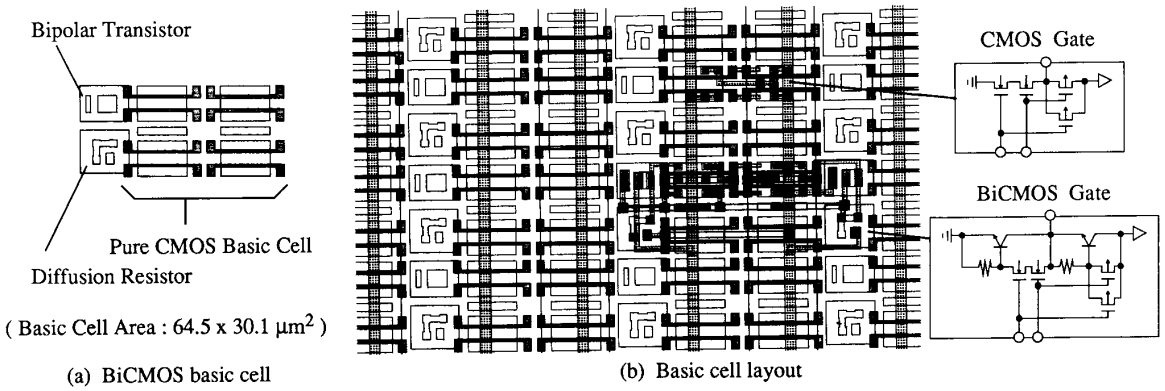


Fig.1 BiCMOS basic cell layout

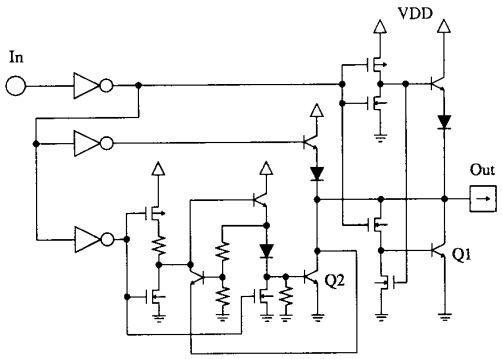


Fig.2 Circuit of TTL output buffer

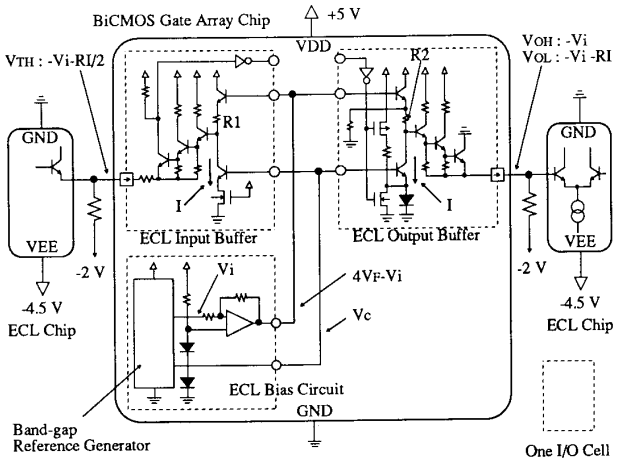


Fig.3 ECL interface scheme

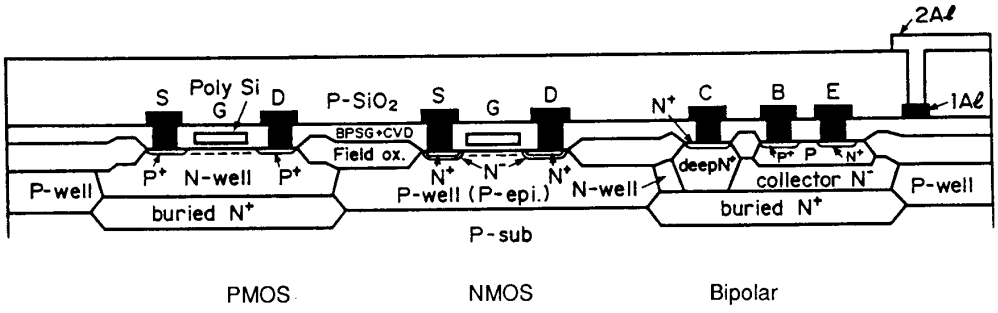


Fig.4 0.8 μm BiCMOS cross-section

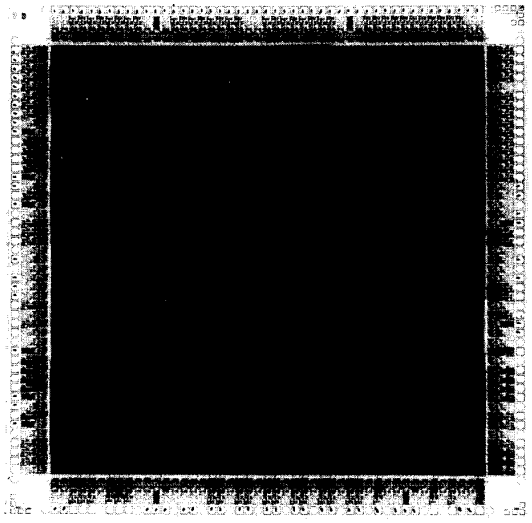
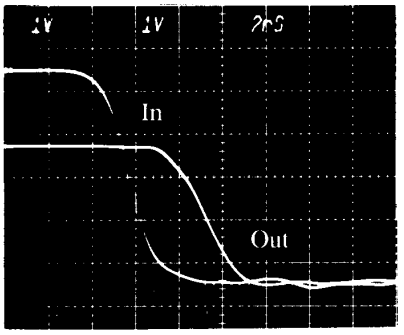


Fig.5 Microphotograph of test chip



(500 Ω / 50 pF Load)

Fig.7 Output waveform of TTL output buffer

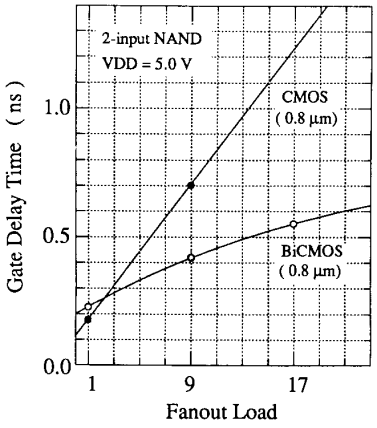


Fig.6 Gate delay time vs. fanout load

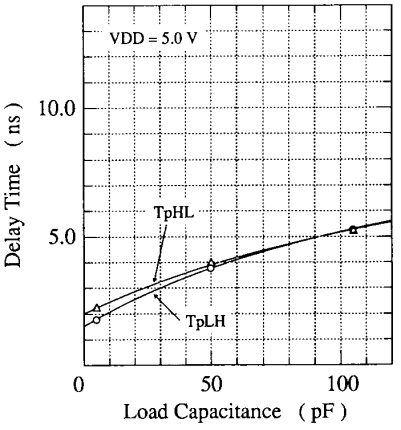


Fig.8 Delay time of TTL output buffer vs. load capacitance

Gate Cells Count	51,012
I/O Cells Count	188
Basic Cell Area	64.5 x 30.1 μm^2
Internal Gate Delay (BiCMOS 2NAND;F.O.=6)	350 ps
Interface Level	CMOS,TTL,ECL
TTL Output Buffer (50 pF Load)	3.8 ns
ECL Output Buffer (50 pF Load)	3.9 ns
Supply Voltage	+ 5 V Single
Chip Size	8.37 x 8.37 mm^2
Process	0.8 μm BiCMOS

Table 1 Performance of 50K 0.8 μm BiCMOS gate array

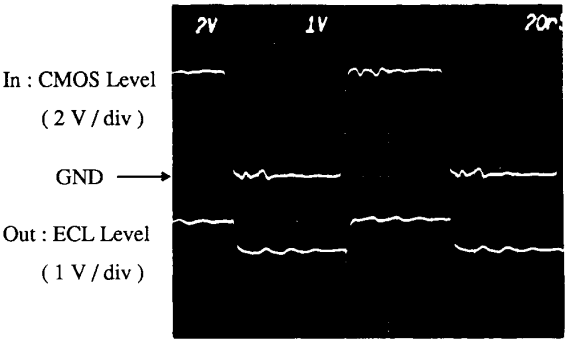


Fig.9 Output waveform of ECL output buffer