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# A Current-Mode Bit-Block Circuit Applicable to Low-Voltage, Low-Power Pipeline Video-Speed A/D Converters

**Yasuhiro SUGIMOTO**†, *Member*, **Shunsaku TOKITO**†, **Hisao KAKITANI**†, *and* **Eitaro SETA**†, *Student Members*

**SUMMARY** This paper describes a study to determine if a current-mode circuit is useful as an analog circuit technique for realizing submicron mixed analog-and-digital MOS LSIs. To examine this, we designed and circuit simulated a new current-mode ADC bit-block for a 3 V, 10-bit level, 20 MHz ADC with a pipeline architecture and with full current-mode approach. A new precision current-mode sample-and-hold circuit which enables operation of a bit block at a clock speed of 20 MHz was developed. Current mismatches caused by the poor output impedance of a device were also decreased by adopting a cascode configuration throughout the design. Operation with a 3 V power supply and a 20 MHz clock speed in a 3-bit A/D configuration was verified through circuit simulation using standard CMOS 0.6 $\mu$m device parameters. Gain error, mismatch of current, and linearity of the bit block with changing threshold voltage of a device were carefully examined. The bit block has a gain error of 0.2% (10-bit level), a linearity error of less than 0.1% (more than 10-bit level), and a current mismatch of DAC current sources in a bit cell of 0.2 to 0.4% (more than 8-bit level) with a 3 V power supply and 20 MHz clock speed. An 8-to 9-bit video-speed pipeline ADC can be realized without calibration. This confirms that the current-mode approach is effective.

***key words:*** *ADC bit-block circuit, current-mode circuit, pipeline-type ADC, video-speed ADC, low voltage, low power*

## 1. Introduction

MOS LSIs should operate at low supply voltages with low power consumption, use submicron devices with low threshold voltages, utilize mainly digital MOS processes in fabrication, adopt parallel processing scheme and realize mixed analog-and-digital functions on the same chip when the LSI design rule decreases significantly below 1 $\mu$m. MOS analog functions on a chip should therefore satisfy these requirements. ADCs and DACs are key elements in analog functions. Video-speed ADCs and DACs in particular should become dominant for picture signal processing in future multimedia equipment. Considering this, many low-voltage and/or low-power video-speed MOS ADCs have been developed [1]-[6]. However, these usually require many capacitors with minimum parasitic capacitance [1]-[6], resistors with good ratio matching, [1]-[4] and many analog switches [1]-[6] in the circuits. This increases their fabrication process complexity, and therefore precludes future MOS LSIs from using a simple digital MOS process. A parallel processing scheme in which low-speed ADCs are used in parallel to realize a high-speed converter has also been proposed [7], [8]. To effectively implement this parallel processing scheme, each ADC should be as compact as possible. A pipeline architecture is considered the best for realizing each ADC in the video signal range. The current-mode approach to a video rate ADC with a pipeline architecture seems to be attractive for eliminating the capacitors, resistors and many switches in the circuit, enabling parallel processing scheme, and obtaining low voltage and low power capabilities. The superior high-frequency, low-voltage operation capabilities of the current-mode and/or switched-current circuit have already been reported [9]. As the current carries information instead of the voltage in these circuits, low-voltage operation is possible because the voltage change in each node is suppressed. High-speed operation is also possible because the impedance of each node is low. Neither does the circuit require capacitors nor resistors in principle. Motivated by superior current-mode circuit features, video rate current-mode ADCs have been developed [10], [11]. The complete elimination of capacitors, switches and resistors can be seen in reference [10]. The superiority of the current-mode approach has been demonstrated. However, Ref. [10] has demonstrated only 8-bit precision, and Ref. [11] uses current-mode circuit only as a part for a 6-bit fine converter adopting a sub-ranging architecture. It still uses a conventional parallel architecture for a coarse ADC and a DAC with capacitors and resistors. As 10-bit precision is expected to be the standard for the video-speed ADCs, it is necessary to demonstrate the true current-mode approach and that such an ADC can be realized in a pipeline architecture. This might suggest the future direction of ADCs and other analog circuits in the sub-micron era. Therefore, we attempted to realize a high-speed, low-voltage, precision video-speed ADC that is most suitable for digital MOS processes and that

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† The authors are with the Department of Electrical and Electronics Engineering, Chuo University, Tokyo, 112 Japan.

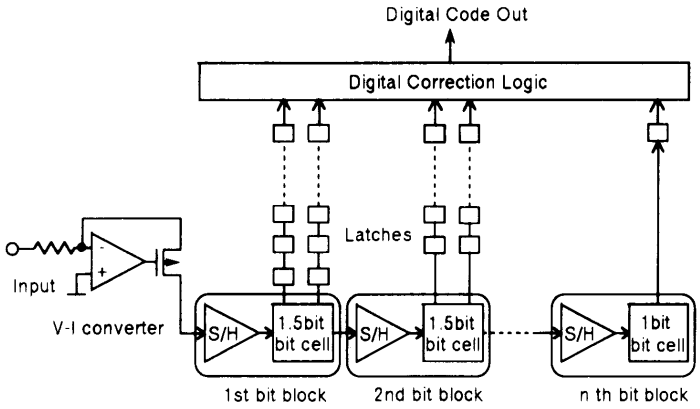



**Fig. 1** New pipelined ADC architecture.

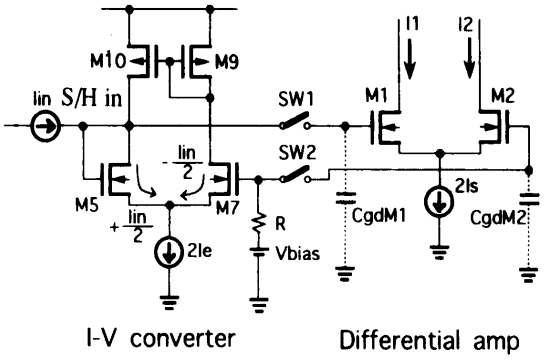
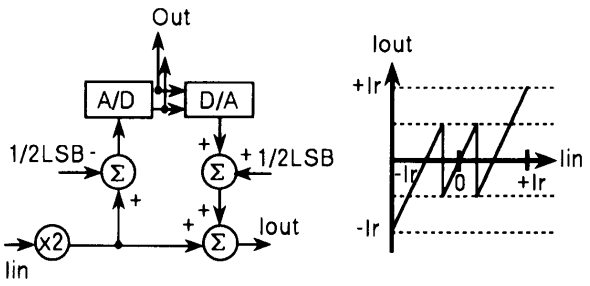



**Fig. 3** Differential sampling scheme.




(a) Block diagram. (b) Input-output current characteristics.

**Fig. 2** 1.5-bit bit cell and its transfer curve.

adopts a pipeline architecture by designing a bit-block circuit with a current-mode circuit. We also examined the influence of parameter variation such as the threshold voltage of a transistor because it seems difficult to obtain good current accuracy in a current-mode circuit. The ADC bit-block circuit is a computer simulated by using 0.6 $\mu$m MOS device parameters in order to clarify limits and possibilities of the current-mode approach. The details will be presented below.

## 2. A New Pipeline ADC Architecture

We have seen that future MOS ADCs might use a parallel architecture. Even in this case, an ADC still needs a larger area because an analog circuit can not be reduced in size proportionally to technological advances and still maintain its performance. The pipeline architecture is very attractive for minimizing the size of high-speed ADCs. It only requires $n$ stages of less than a 2-bit small bit block. Some current-mode ADCs have been designed with a pipeline architecture [12], [13]. Although 8-bit [12] and 10-bit [13] resolutions were obtained, their conversion speeds were limited to 1.75 $\mu$s [12] and 550 kHz [13] because the decision in each bit block in the pipeline is not performed at the clock speed. Those converters wait until the decisions of all the bit blocks connected in series are made. To improve the speed of previous pipeline ADCs, a new high-speed, high-precision sample-and-hold circuit is placed in front of each bit cell as shown in Fig. 1. This enables each bit block to operate at the clock speed. Our objective is to study the current-mode circuit realization of the bit block that is directly applicable to a pipeline ADC featuring a 3 V supply voltage, 20 MHz clock frequency, and 10-bit resolution. Each bit cell in Fig. 1, except for the $n$-th bit cell, has a resolution of 1.5 bits utilizing the digital correction scheme, which means that it contains only two comparators. The block diagram and its input-output current characteristics are shown in Fig. 2. This 1.5-bit bit cell concept is from Ref. [14] and is widely acknowledged as an effective means to construct a pipeline ADC. Digital correction is necessary because we use a 0.5-bit redundant bit. Latches are inserted so that the result from each bit cell reaches the digital correction logic at the same time. For a sample-and-hold circuit and a bit cell in the first bit block, 10-bit linearity and accuracy of current gain is needed. This requires a sophisticated design for these circuits.

## 3. Circuit Design of Bit Block, Input, and Digital Correction Circuits

### 3. 1 Sample-and-Hold Circuit

The first stage sample-and-hold circuit should realize 10-bit linearity and gain accuracy at a clock rate of 20 MHz. Although the constant offset of current at the output is corrected by the digital correction circuit, the conventional current-mode circuit can not guarantee the linearity and small gain error because of the voltage change at the gate terminal due to the charge feed-through from analog switches and poor output impedance of the device [15], [16]. A new differential switching scheme was developed to achieve good linearity and gain accuracy while avoiding feed-through and offset in the video frequency. This scheme features the minimum number of switches which operate at a voltage of VDD/2, effective cancellation of clock feed-through, and symmetrical current mirroring with high output impedance. The basic idea of this

sample-and-hold operation is shown in Fig. 3. Transistors M5, M7, M9, M10 and a current source $2Ie$ compose a current to voltage ($I$-$V$) converter with a feedback loop, and transistors M1, M2 and a current source $2Is$ compose a differential amplifier. When input current Iin is applied to the $I$-$V$ converter, current change of $+Iin/2$ ($-Iin/2$) occurs for currents flowing through M5 (M7). As currents flowing through M5 and M7 are mirrored to currents flowing through M1 ($I1$) and M2 ($I2$), the input current $Iin$ is reproduced by the difference current $I1-I2$. More precisely,

$$Iout = I1 - I2 = Iin \times \sqrt{1 + \frac{4}{Iin^2}(Is - Ie)(2Ie - \sqrt{(2Ie)^2 - Iin})} \quad (1)$$

When $Is = Ie$, $Iout$ becomes exactly equal to $Iin$. If we can assume that $(Iin/2Ie)^2$ is small compared with 1, then Eq. (1) can be approximated to

$$Iout \fallingdotseq Iin\sqrt{\frac{Is}{Ie}} \quad (2)$$

Equation (2) shows that current gain ($Iout/Iin$) is proportional to the root of the current ratio of $Is$ to $Ie$. The influence of the ratio change of $Is$ to $Ie$ is reduced. Using this fact, we can calibrate current gain by intentionally changing the current ratio. For the sample-and-hold circuit, two analog switches are inserted between an $I$-$V$ converter and a differential amplifier. Impedances and capacitor values seen from switches are set equal for symmetrical operation. $R$ shown in Fig. 3, which is the output impedance of a source follower, is equal to the impedance at terminal S/H in. As error voltages due to feed-through of switches appear equally at the gates of M1 and M2, they are suppressed at the output by the common-mode rejection characteristic of a differential amplifier when $I1 - I2$ is taken. To compensate for the small peak in the $I$-$V$ converter frequency characteristic caused by a feedback loop, small capacitors CgdM1 and CgdM2, which are composed gate to source and drain capacitance of a transistor, are added. Another thing to be considered is the poor output impedance of a transistor. Drain-to-source voltage change of a transistor usually causes errors for the ratio of a current mirror. Cascode connection of transistors is useful for eliminating this effect. The overall schematic of the high-precision sample-and-hold circuit is shown in Fig. 4. As the voltage at terminal S/H in is VDD/2, the voltage at the source and drain terminals of the switching transistors becomes VDD/2. When the switch is turned off, the gate-to-source voltage is reverse biased to $-$VDD/2, thus ensuring complete cut off of switches even when low threshold transistors are used. This configuration avoids the leakage problem for low threshold transistors [17]. The minimum supply voltage of a sample-and-hold circuit is estimated to be $2V_{th}+4\Delta$, where $\Delta$ is a few hundred millivolts necessary for ensuring the transistor operates in the saturation region. When $V_{th}=0.4$ V, it is 1.6 V [18]. In Fig. 4, the full-scale input signal current is $\pm 20\ \mu$A and is applied to the S/H in terminal. The capacitance of CgdM1 and CgdM2 is 0.3 pF. The output has a folded cascode configuration and subtracts currents in M1 and M2. Switch feed-through is canceled and output impedance is increased. More than 10-bit output current linearity can thus be obtained.

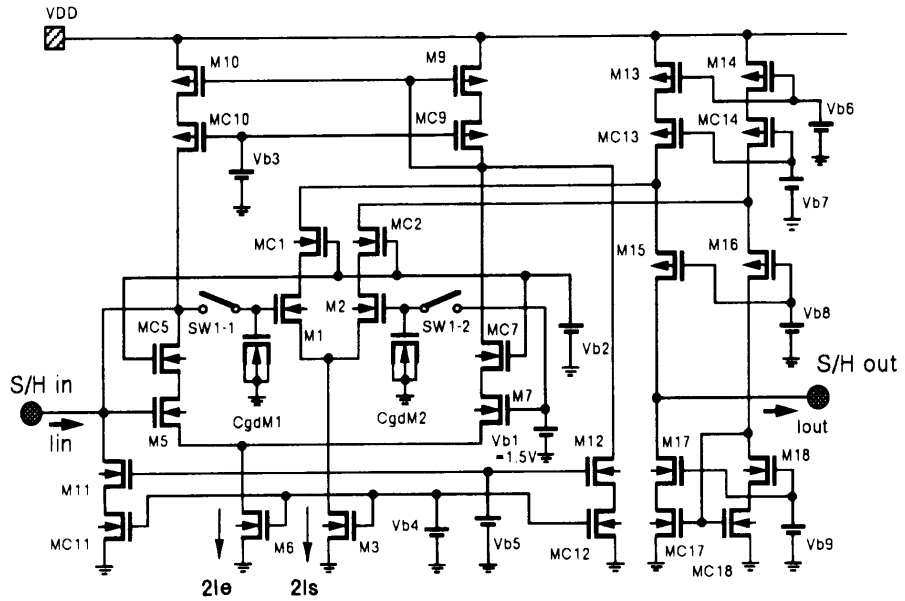



**Fig. 4** Sample-and-hold circuit.

### 3. 2 Bit Cell Circuit

The output current of a sample-and-hold circuit is fed to the 1.5-bit bit-cell circuit shown in Fig. 5. The circuit produces the output current shown in Fig. 2(b). The sample-and-hold circuit reverses its input current, and the characteristic of the 1.5-bit bit cell is the reverse of that in Fig. 2(b). The input current is doubled by the current mirror which consists of Ma3, Ma5 and Maa5. The doubled current is applied to current comparators Comp1 and Comp2 through current mirrors Mc3, Mc4 and Mc5. *Iin* is $\mp 20\ \mu$A when an input current of $\pm 20\ \mu$A is applied to the sample-and-hold circuit. At the same time, a 100 $\mu$A constant offset current is applied to terminal *Iin*. The doubled current flowing through Mc4 and Mc5 becomes 200 $\mp 40\ \mu$A. As *Icp*1 is set to $+190\ \mu$A and *Icp*2 to $+210\ \mu$A, Comp1 (Comp2) changes state when *Iin* reaches $-5\ \mu$A ($+5\ \mu$A). The doubled input current is also fed to the *Iout* terminal through the current mirror Ma7 and Maa7. Constant current *Ioff* of $+180\ \mu$A is applied to the *Iout* terminal, producing $+20\ \mu$A to $-60\ \mu$A of current at the *Iout* terminal if comparators don't change. When *Iin* reaches $-5\ \mu$A, the current at *Iout* terminal decreases to $-10\ \mu$A. Comp1 changes state and activates Md4, which forms a current switch with Md5. This adds $+20\ \mu$A of current to the *Iout* terminal through the constant current source *Ida*1, and the current at the *Iout* terminal skips to $+10\ \mu$A. When *Iin* is increased to $+5\ \mu$A, the same kind of action occurs, and $+20\ \mu$A of *Ida*2 current is added again to the *Iout* terminal. Note that the comparator status change is not strictly controlled because it will be corrected digitally by the digital correction logic. The minimum supply voltage of the 1.5-bit bit cell is calculated to be $2V_{th}+2\Delta$, which is smaller than that of a sample-and-hold circuit. The voltage of both input (*Iin*) and output (*Iout*) terminals is VDD/2.

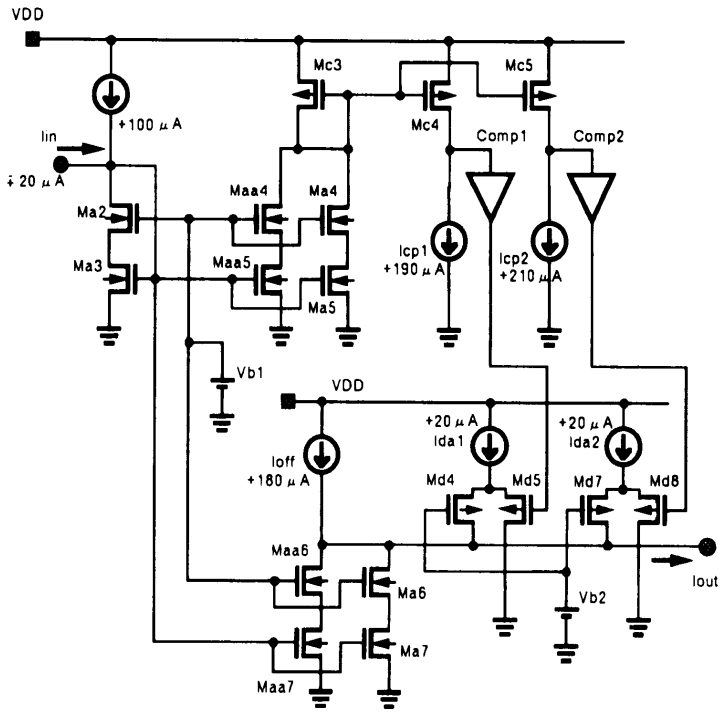



**Fig. 5** 1.5-bit bit cell circuit.

### 3. 3 Input and Digital Correction Circuits

The input signal for an ADC is usually in the form of voltage. Therefore, it is necessary to convert the signal voltage into signal current for input to the current-mode ADC. The input circuit shown in Fig. 6 will be used. In Fig. 6, operational amplifier *OP*1, resistor *Rin*, transistor *Me* (or *Qe*) and current sources *Is*1 and *Is*2 are external, while current mirrors are internal to the ADC. *Is*1 and *Is*2 are selected to be equal, and only signal current flows in to and out from the first stage sample-and-hold circuit. A digital correction

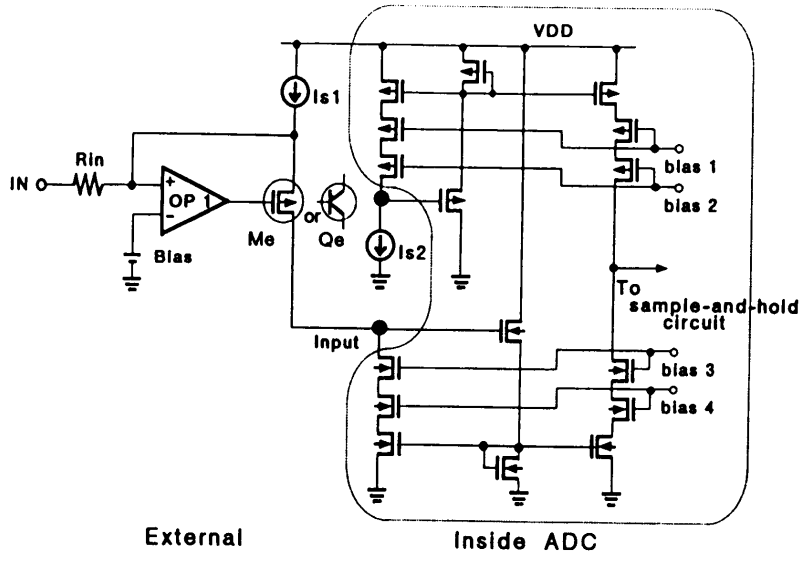



**Fig. 6** ADC input circuit.

scheme is also adopted to relax the criteria for dynamic range in each bit block and the comparator's threshold change. However, the digital correction circuit has already been described in Ref. [19] and will not be described in this paper.

## 4. Requirements for Gain Error and Current Matching

To obtain 10-bit accuracy, tight performance criteria are posed for the converter first stage cell circuit. The DAC in a bit cell (*Ida*1 and *Ida*2 in Fig. 5) and gain error should have 10-bit accuracy to maintain good characteristics of differential nonlinearity (DNL) and integral linearity (INL). The bit-block circuit uses numerous current mirrors. Current mirrors may introduce a ratio matching error due to the variation of device parameters such as transistor threshold voltage. The constant offset, except for current sources in a bit cell of DAC, introduced by this mismatch does not affect the overall performance of the ADC as long as it is within the correction range of the digital correction. In order to clarify the requirement for the gain error, the allowable gain error of the first-stage cell circuit is examined. The relationship between *Iout* and *Iin* in the first-stage bit block without folding is illustrated in Fig. 7 where gain change is denoted by $\Delta G$. Even when currents are folded, the overall gain error does not change and becomes maximum at the far end of the transfer curve in Fig. 7. Thus, maximum gain error becomes $\Delta G \times Iin$. As *Iin* and *Iout* are bidirectional currents, $G$ is amplified based on half the input current. The equivalent error current at input then becomes $(\Delta G/G) \times Iin$, and this should be accurate to within 10 bits of the full scale current of $2Iin$. When $n$ denotes the number of stages of the A/D converter, then

$$\frac{\Delta G}{G} \times Iin = \frac{2Iin}{2^n} \tag{3}$$

is obtained. Substituting 2 for $G$ and 10 for $n$ yields

$$\Delta G/G = 0.002 = 0.2\% \tag{4}$$

The possible sources of gain error are considered the current change between *Ie* and *Is*; $V_{th}$ variation of differential transistors M1, M2, M5 and M7; variation of capacitor values of CgdM1 and CgdM2 in Fig. 4; and the gain change in the current mirror such as Ma3, Ma7 and Maa7 in Fig. 5. Any offset current within the correction range of $\pm 5\ \mu$A is corrected. It is also unnecessary for the comparator to have the exact gain or small offset. However, the DAC currents *Ida*1 and *Ida*2 in Fig. 5 should have the 10-bit accuracy. The influence of parameter changes on the gain error, linearity and bandwidth of the sample-and-hold amplifier will be examined later by circuit simulation. As a 1.5-bit bit cell consists mainly of current mirror circuits, we studied the accuracy of the current ratio of the simple current mirror circuit in Fig. 8. Assume that transistors M1 and M2 are the same size, that the drain-to-source voltages of input and output transistors are the same, and that they are in saturation. Then input current is approximated as

$$Iin = \frac{\beta}{2}(V_{GS} - V_{th})^2 \tag{5}$$

Now, the output transistor M2 has a $V_{th}$ variation of $+\Delta$ relative to input transistor M1. Then, the output current is

$$Iout = \frac{\beta}{2}(V_{GS} - V_{th} - \Delta)^2 \tag{6}$$

Where $\beta = KW/L$, $K$ is the transconductance parameter and $V_{GS}$ is the gate-to-source voltage of M1 and M2 (in this case, it is $V$). Calculating $(Iin - Iout)/Iin$ from Eqs. (5) and (6) yields

$$\frac{Iin - Iout}{Iin} \doteqdot \frac{2\Delta}{V_{GS} - V_{th}} \tag{7}$$

Equation (7) shows that, for a first order approximation, current mismatch is proportional to twice $V_{th}$ variation and inversely proportional to $(V_{GS} - V_{th})$. It

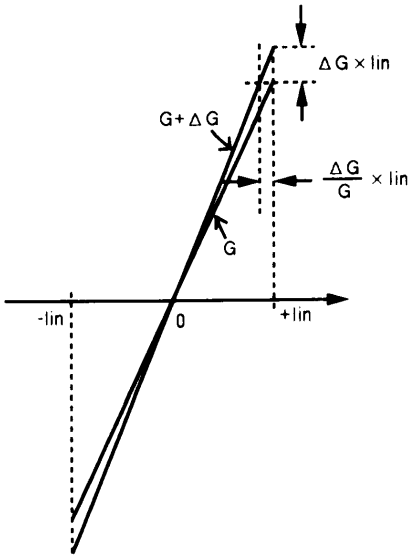



**Fig. 7** Gain error estimation.

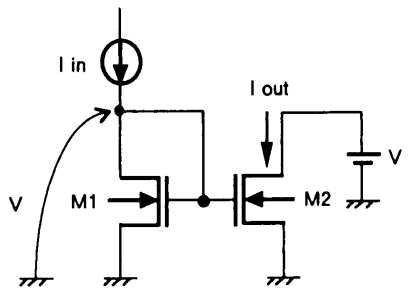



**Fig. 8** A simple current mirror circuit.

is evident that $(V_{GS}-V_{th})$ must be large in order to reduce mismatch. As supply voltage becomes low in sub-micron devices, it is difficult to have large $(V_{GS}-V_{th})$ in general and current mismatch is expected to increase.

## 5. Simulation Results

To verify that the bit-block design applies to a 3 V, 20 MHz pipeline ADC, we simulated a 3-bit configuration, the block diagram of which is shown in Fig. 9, by SPICE circuit simulation. Device parameters used are from conventional 0.6 $\mu$m CMOS processes. Threshold voltage $(V_{th})$ for PMOS (NMOS) is $-0.85$ V (0.85 V). For switching transistors in the sample-and-hold circuit, $V_{th}$ for PMOS (NMOS) is $-0.2$ V (0.2 V). In Fig. 9, two 1.5-bit bit block stages plus a 1-bit A/D bit block produce the 3-bit output. Latches are used to synchronize all comparator outputs. A digital correction circuit is also incorporated. Figure 10 shows the input and output waveforms of a first stage sample-and-hold circuit with 3 V power supply, 20 MHz clock and $\pm 20$ $\mu$A input current of 1 MHz. The current difference between adjacent hold values is measured to check linearity. It ranges from 4.003 $\mu$A to 4.006 $\mu$A, indicating just 3 nA change, that is, less than 0.01% of linearity. Figure 11 shows the simulation result of the input current waveform and its corresponding digital outputs in the 3-bit configuration shown in Fig. 9 with a 3 V power supply,

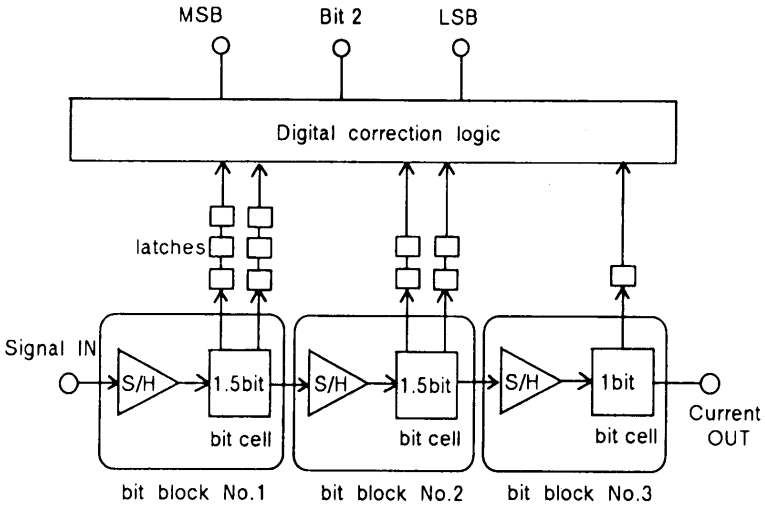



**Fig. 9** 3-bit A/D converter simulated with SPICE.

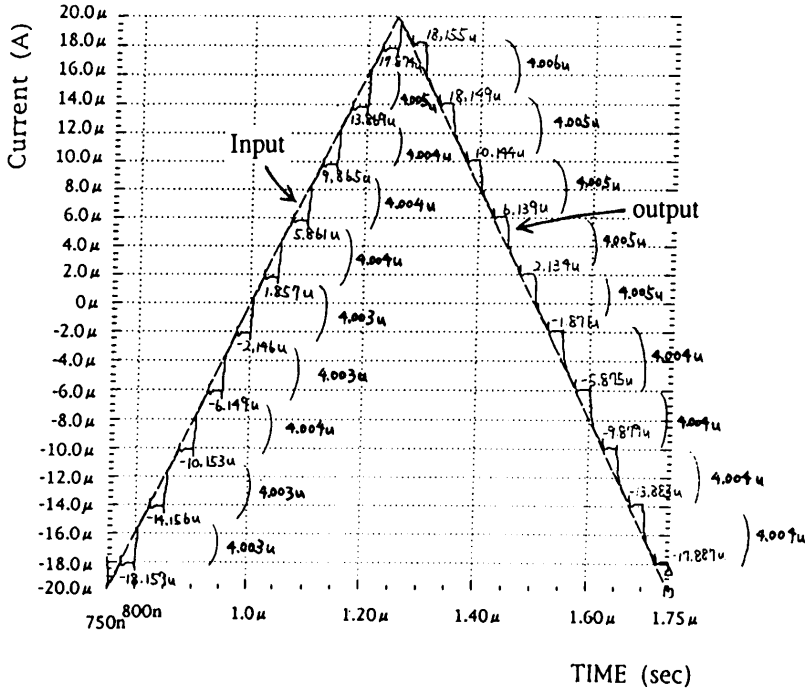



**Fig. 10** Input and output current waveforms of a sample-and-hold circuit (VDD 3.0 V, Clock 20 MHz, *Iin* 1 MHz).

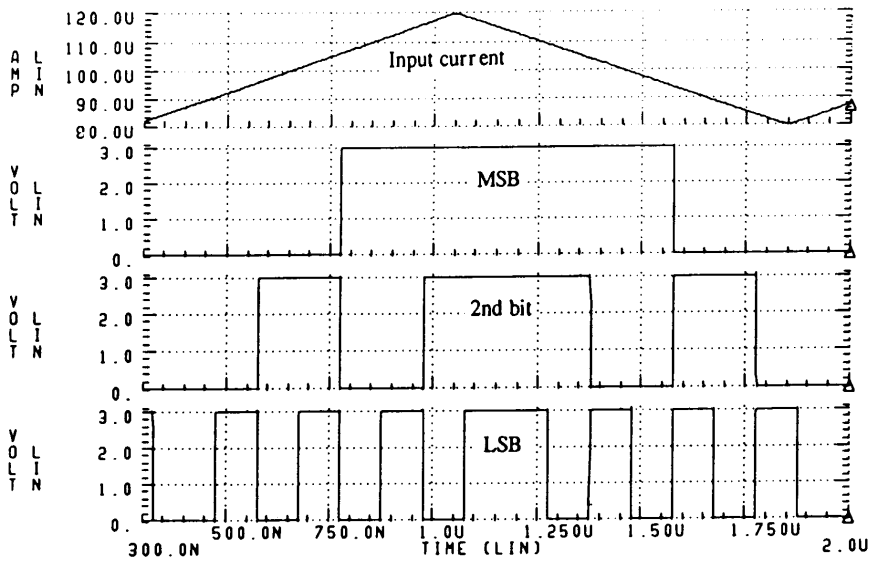



**Fig. 11** Simulation result of circuit in Fig. 9 (VDD 3.0 V).

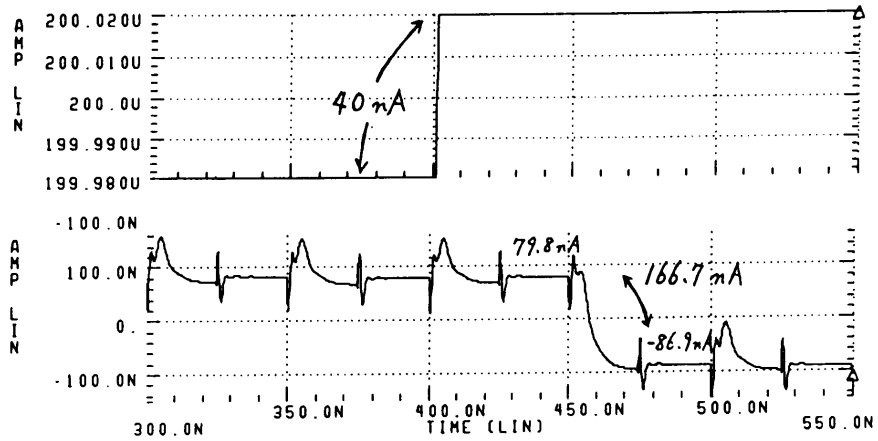



**Fig. 12** Simulation result of circuit in Fig. 9 for a small step change of input current (VDD 3.0 V).

20 MHz clock and $\pm 20\ \mu$A input current of 1 MHz. The output data is delayed by 2.5 clock periods relative to the input signal sampling instance. Figure 11 indicates the correct operation of the circuit. Figure 12 shows the output current change at the output of the sample-and-hold circuit in the third bit block when a 40 nA (1/1000 of full-scale input) input current change at the middle level is applied to the input of this 3-bit A/D converter. The current change should ideally become 160 nA. Currents are subtracted both in the first 1.5-bit bit block and the second 1.5-bit bit block in this case. As the error does not increase to 1/2 of the current change at the output, it is possible to extend this circuit configuration to 10 bits in this ideal case. Next, we will examine the influence of parameter changes. All the simulation is carried out with 3 V supply voltage if not otherwise specifically stated. Figure 13 shows the gain error with a 1 MHz input signal at the output of a sample-and-hold amplifier in sample mode when the current of M3 ($2Is$) and that of M6 ($2Ie$) in Fig. 4 changes. As indicated in Eq. (2),

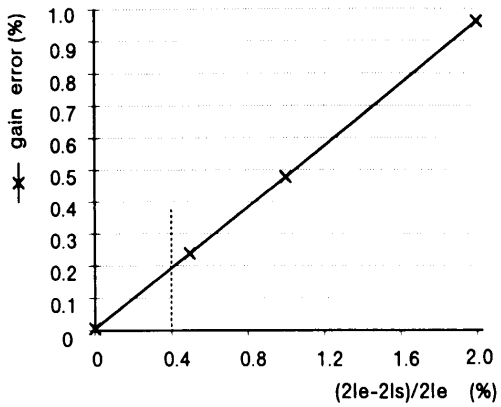



**Fig. 13** Gain error caused by mismatch of $Is$ and $Ie$.

this current mismatch causes a gain error. A 0.4% mismatch results in a 0.2% gain error which is the limit for the 10-bit accuracy. The linearity error is less than 0.01% for the change of 0 to 2% of $(2Ie\text{-}2Is)/2Ie$ in this case. Figure 14 shows the gain error and the $-3$ dB frequency of a sample-and-hold circuit when the

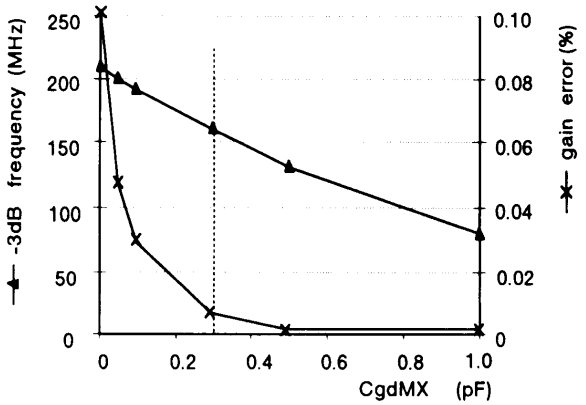



**Fig. 14** Gain error and −3 dB frequency dependence on CgdM1 and CgdM2.

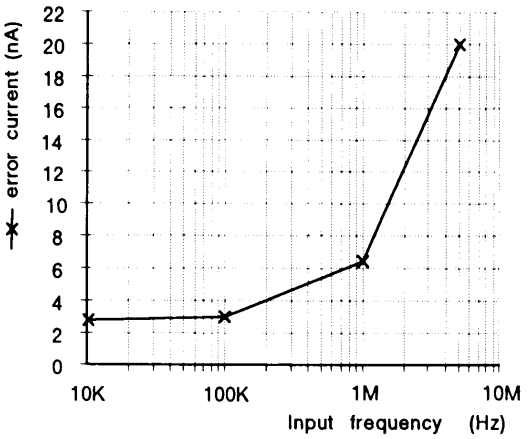



**Fig. 15** Input frequency versus error current characteristic.

capacitor value of CgdM1 and CgdM2 changes. The −3 dB frequency is simulated in the sample mode while gain error is simulated in sample-and-hold mode with a 1 MHz input signal. In addition to a small imbalance of switch feed-through, there exists a small peak in the frequency characteristic of the $I$-$V$ converter in Fig. 3. The peak produces the gain error, and these capacitors effectively compensate for it. A 0.3 pF of capacitor value is chosen at the point the gain error decreases below 0.01%. Figure 15 is the input signal frequency vs. error current characteristic at the output in sample mode when the capacitor value is 0.3 pF. The switch-on resistance modulated by the input signal produces a nonlinear time constant together with the capacitor. This causes a frequency dependent error current. The error is only 0.05% (full scale is 40 $\mu$A) when a 5 MHz input signal is applied. Variations of capacitances of CgdM1 and CgdM2 (2% change) and of switch transistor size (double and triple) were also simulated, however no notable change in gain error (less than 0.04%) or linearity error (less than 0.003%) was observed. Figure 16 shows the gain error and offset at the output terminal of a sample-and-hold circuit in the sample-and-hold operation when $V_{th}$ of transistor M1 of a differential amplifier in Fig. 4

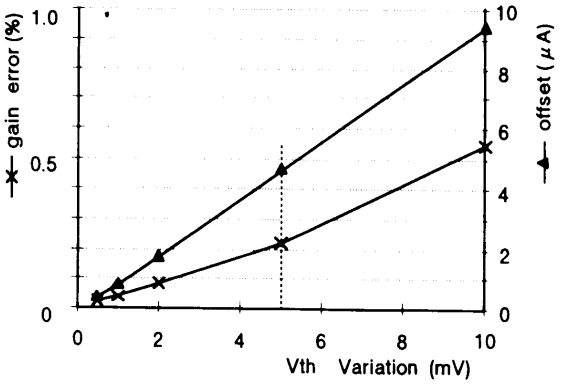
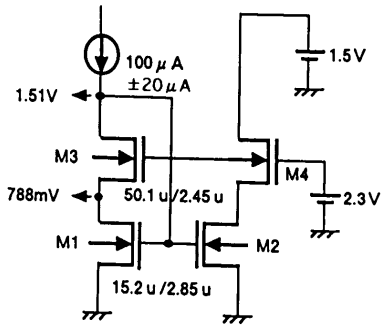
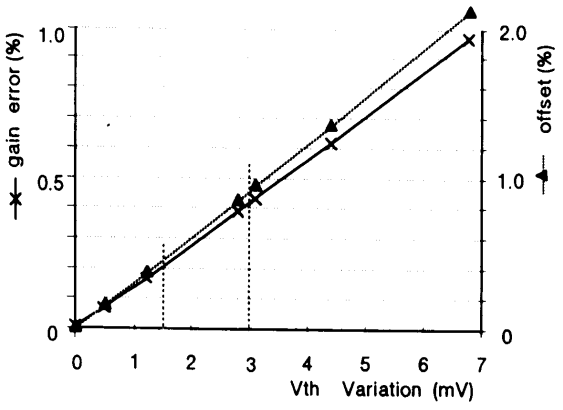



**Fig. 16** The influence of the $V_{th}$ variation of a differential pair.




(a) Current-mirror circuit.

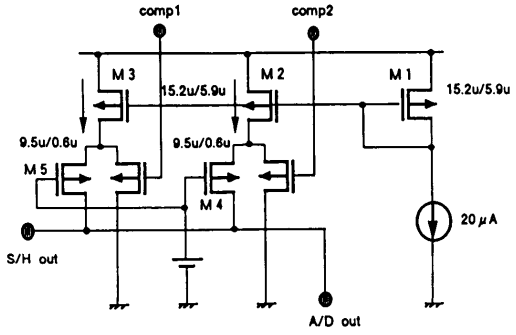



(b) Gain error and offset.

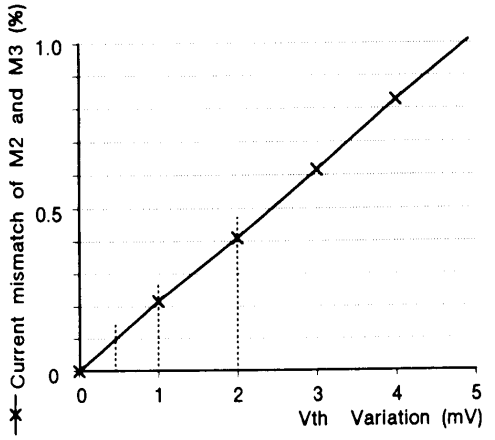
**Fig. 17** The effect of the current-mirror mismatch.

changes. Although the offset current at the output increases due to the imbalance of a differential pair, the gain error is less than 0.25% when the $V_{th}$ variation is 5 mV. Offsets of less than 5 $\mu$A are corrected by digital correction. A linearity error, which is not shown in the figure, was also simulated with a 10 mV $V_{th}$ change and only the less than 0.02% of error was observed. More simulations were carried out to see the influence of the $V_{th}$ change and the supply voltage change. In case when $V_{th}$s of transistors M1 and M2, or M1 and M5 change simultaneously by the same amount of 10 mV relative to M5 and M7, or M2 and M7 in Fig. 4, respectively, both linearity and gain error are less than

0.01%. As the sample-and-hold circuit is symmetric, $V_{th}$ changes of those transistors do not affect the performance. For a supply voltage change of ±5%, that is 2.85 to 3.15 V, without changing $V_{th}$ of transistors, the linearity error is less than 0.04% and the gain error is less than 0.01%. From these data, we can conclude that the mismatch of $2Is$ and $2Ie$ only affects the gain error ; the linearity is always good. Figure 17 is the offset and the gain error of a current mirror in a 1.5-bit bit cell when $V_{th}$ of the mirror transistor changes. Figure 17(a) is the simulated circuit and Fig. 17(b) shows its characteristics. Input current is 100± 20 $\mu$A. The size of current mirror transistors M1 and M2 is identical in this case. When the current ratio is 2, the offset should double, however, gain error in percentage does not change. This gain error directly affects the overall performance of the ADC. For the first-stage bit cell of a 10-bit ADC, this error should be less than 0.2%. In the figure, this equals a $V_{th}$ change of 1.5 mV. We have already seen that current mismatch between $2Is$ and $2Ie$ in Fig. 4 causes the gain error. The total gain error in the bit block becomes the sum of the error of a sample-and-hold circuit and the error of a current mirror in Fig. 17(a). Although careful layout design and selection of transistor size help suppress the $V_{th}$ variation of transistors, less than 1.5 mV $V_{th}$ change is still a little bit difficult to realize. It is satisfactory, however, to adjust the gain error in total in a bit block. It might be useful to change the current value of $2Is$ or $2Ie$ by incorporating a calibration method to ensure 10-bit accuracy. If 9-bit accuracy is enough, then the criteria is relaxed to about 3 mV of $V_{th}$ change. The major problem resides in the DAC current sources. DAC current source mismatch is simulated in Fig. 18. Figure 18(a) shows the DAC circuit in a bit cell and Fig. 18(b) shows mismatch current in percent when $V_{th}$ of M2 and M3 changes. The current value of M2 and M3 is 20 $\mu$A, and 0.1% of accuracy is expected for 10-bit accuracy. However, the data says, less than 0.4 mV of $V_{th}$ change is required for M2 and M3. This is difficult to achieve, so some calibration method is necessary. If 9-bit accuracy is required, the $V_{th}$ change is relaxed to 1 mV, and for 8-bit accuracy to 2 mV. A practical calibration circuit has not been examined yet. This is left for further study. Figure 19 is the settling time of comparator Comp 1 and DAC differential switch Md4 and Md5 in Fig. 5 when signal current changes from 189 $\mu$A to 195 $\mu$A. The sink current of $Icp1$ in Fig. 5 is 190 $\mu$A. The settling time is measured from the time a comparator




(a) DAC circuit in a bit cell.




(b) Current mismatch with $V_{th}$ variation.

**Fig. 18** Current mismatch characteristic of the DAC in a bit cell.

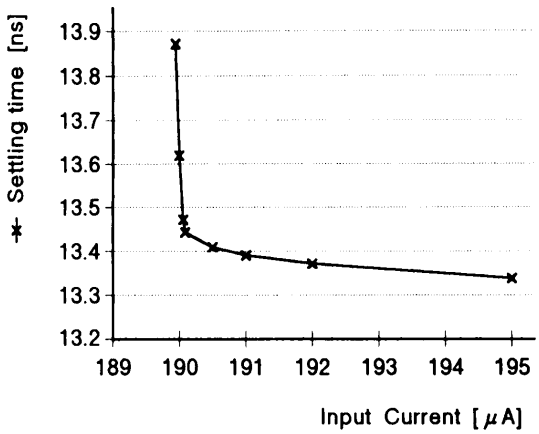



**Fig. 19** DAC settling time.

**Table 1** Overall circuit performance of the bit-block circuit.

| Items | | Values |
|---|---|---|
| Threshold votage | NMOS | +0.85 V |
| | PMOS | −0.85 V |
| Switching transistor | NMOS | +0.2 V |
| | PMOS | −0.2 V |
| Input current | | ±20 μA |
| Sampling frequency | | 20 MHz |
| -3dB bandwidth of a sample-and hold-circuit | | 160 MHz |
| Capacitor value (CgdM1,CgdM2) | | 0.3 pF |
| Linearity of a sample-and-hold circuit | | less than 0.01% (1MHz input) |
| Acquisition time of a sample-and-hold circuit (0.1%) | | 16 nS |
| Power supply | | 3 V |
| Current dissipation of a sample-and-hold circuit | | 700 μA |
| Current dissipation of a 1.5-bit bit cell | | 900 μA |

strobe is activated to the time current at the *Iout* terminal settles within 20 nA of the desired value. There is about 10 mV uncertainty at input of the comparator. However, this is not the problem. The DAC current settles well within the half clock time of 20 MHz. Table 1 summarizes the performance of this bit-block circuit. As each sample-and-hold circuit and 1.5-bit bit-cell contains a bias circuit, current consumption becomes large. The bias circuit can be used in common when many bit-block stages are used on a chip.

## 6. Conclusion

We have studied a low-supply-voltage, low-power 10-bit level video-speed pipeline ADC with a full current-mode approach through the design and circuit simulation of a bit-block circuit to demonstrate the possibility for realizing future mixed-mode MOS LSIs in sub-micron devices. We confirmed 3 V operation and 20 MHz clock speed without using sophisticated capacitors, resistors or many analog switches. The $V_{th}$ mismatch of transistors in DAC current sources in the bit block becomes the most critical matter and the gain error caused by the current mismatch of a current mirror in a 1. 5-bit bit-cell becomes the next critical matter to obtain 10-bit accuracy. For the 10-bit realization, only 0.4 mV $V_{th}$ change for transistors of current sources in DAC and 1.5 mV change for transistors in the current mirror in 1.5-bit bit-cell are allowed. This is relaxed to 1 mV and 3 mV for the 9-bit realization and 2 mV and 5.5 mV for the 8-bit realization. A calibration method should be incorporated for the 10-bit realization. This is left for future study. It was also implied that voltage operation below 2 V is possible. We can conclude that current-mode approach is effective as an analog circuit technique for application to the future mixed-mode MOS LSIs in sub-micron devices.

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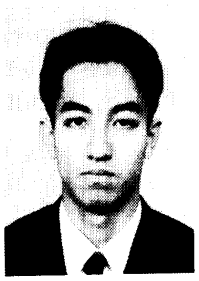
**Yasuhiro Sugimoto** received the B.E. degree from Tokyo Institute of Technology, Tokyo, Japan, M.E. degree from University of Michigan, Ann Arbor, Michigan, and Doctor of Engineering degree from Tokyo Institute of Technology, Tokyo, Japan, in 1973, 1980, and 1991, respectively. He joined Toshiba Semiconductor Group in 1973, and engaged in the development of analog VLSIs. Since 1992, he has been with the Faculty of Science and Engineering, Chuo University where he is now a professor in the Department of Electrical and Electronic Engineering. His main interest is the design and development of new circuits in mixed analog and digital VLSIs. He is the recipient of the 1990 Best Paper Award of European Solid-State Circuits Conference. He is the author of two books. Dr. Sugimoto is a member of the Institute of Electrical and Electronics Engineers, the Institute of Electrical Engineers of Japan and the Japan Consulting Engineers Association.



**Shunsaku Tokito** was born in Hiroshima, on September 30, 1971. He received the B.E. degree in electrical engineering from Chuo University, Tokyo, Japan in 1994. Since 1994, he has been with the Graduate School of Electrical and Electronics Engineering, Chuo University. His main interest is in CMOS analog circuits, especially in analog to digital converter circuits. Mr. Tokito is a student member of the Institute of Electrical and Electronics Engineers of Japan.

**Hisao Kakitani** was born in Tokyo, on October 28, 1971. He received the B. E. degree in electrical engineering from Chuo University, Tokyo, Japan in 1994. Since 1994, he has been with the Graduate School of Electrical and Electronics Engineering, Chuo University. His main interest is in CMOS analog circuits, especially in analog to digital interface circuits. Mr. Kakitani is a student member of the Institute of Electrical and Electronics Engineers of Japan.

**Eitaro Seta** was born in Tokyo, on August 15, 1971. He received the B.E. degree in electrical engineering from Chuo University, Tokyo, Japan in 1995. Since 1995, he has been with the Graduate School of Electrical and Electronics Engineering, Chuo University. His main interest is in CMOS analog circuits design. Mr. Seta is a student member of the Institute of Electrical and Electronics Engineers of Japan.