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A Study of a MOS VCO Circuit by Using a Current-Controlled Differential Delay Cell

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SUMMARY A MOS VCO which has improved linearity of oscillation frequency versus control voltage and has no 1/2 divider is studied. The improved VCO characteristic has been obtained by the use of only two additional transistors, one of which has a role of a load and another of which has a role of a control current source in a differential type delay cell.

key words: *MOS analog circuit, PLL, VCO, current control, differential delay cell*

1. Introduction

Integrated phase-locked loops (PLLs) have been widely used for application on microprocessors. A voltage controlled oscillator (VCO) is a key element in the PLL. But some of the conventional PLL circuits lack in the linearity of the frequency characteristic [1] and require a 1/2 divider [1], [2], and the other needs complex circuits [2]. To realize a simple VCO circuit with an improved linearity and a 50% of duty, a current-controlled differential delay cell is studied. The result is a proposal of a new VCO circuit. Details including simulation results are described in this paper.

2. The Characteristic of a Commonly Used VCO Circuit

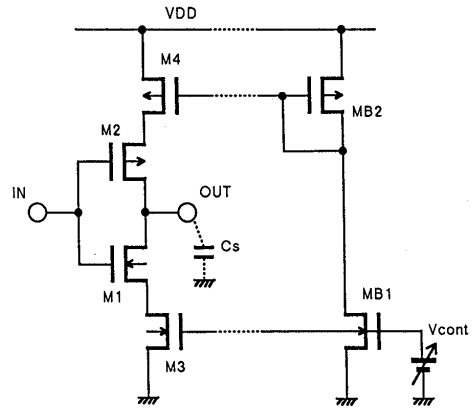
Non-linear characteristic of a commonly used VCO circuit is shown first. Figure 1 (a) is a circuit of a delay cell. A VCO consists of an odd number of delay cells connected in series. A 50% of duty is hard to obtain because of the different delays in rising and falling edges. Figure 1 (b) shows the SPICE simulated characteristic of the oscillation frequency versus control voltage. The frequency change in the low control voltage region is greater than that in the high control voltage region. The curve is non-linear and it is not suitable for VCO. Analysis shows that transistors M3 and M4 change their states from being as current sources to variable resistors when the control voltage changes from low to high.

3. Analysis of a Differential Type Delay Cell

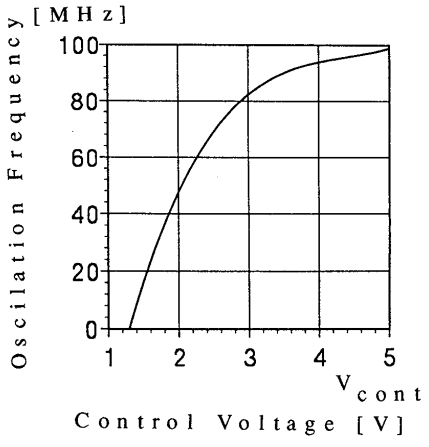
A 50% of duty is guaranteed by the use of a differential type delay cell [2]. Figure 2(a) shows this circuit. Each cell has load capacitors labeled C_s, which are input capacitors of the next cell. When step inputs are applied to the input terminals, output voltage rise and fall by the time constant $R_L C_s$ as shown in Fig. 2(b). The delay t_d is the time from an input change to the time when two curves cross. That is,

$$t_d = R_L C_s \ln 2 \quad (1)$$

The oscillation frequency of a VCO is inversely proportional to the time t_d. Equation (1) tells that if R_L is inversely proportional to the control current, the frequency change becomes linear. This condition is described as,



(a) A delay cell circuit.



(b) Frequency vs. control voltage characteristic.

Fig. 1 A commonly used VCO circuit.

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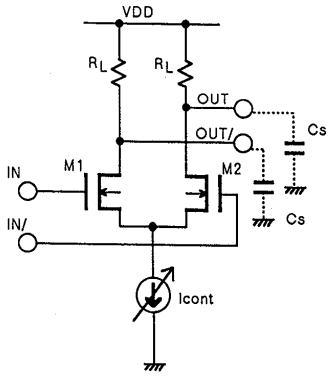
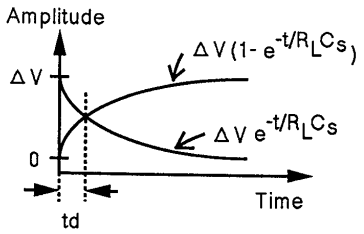


(a) A delay cell circuit.



(b) The delay of a cell.

Fig. 2 A differential type delay cell.

$$R_L I_{cont} = \Delta V = \text{constant} \tag{2}$$

However, the circuit becomes too complex to realize the condition in Eq. (2)[2].

4. A New VCO Circuit and Its Characteristic

A simple circuit that shows the same performance as described above is desired. When a load resistor is replaced by a transistor as shown in Fig. 3(a), the value of an equivalent resistor R_{Leq} becomes,

$$R_{Leq} = 1/g_m \tag{3}$$

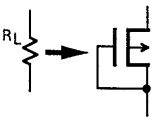
where, $g_m = \sqrt{2\beta_P I_{cont}}$, and β_P is the transconductance parameter of a PMOS transistor.

This makes frequency change proportional to the root of I_{cont}. It also implies if an NMOS transistor is used for supplying I_{cont}, that is,

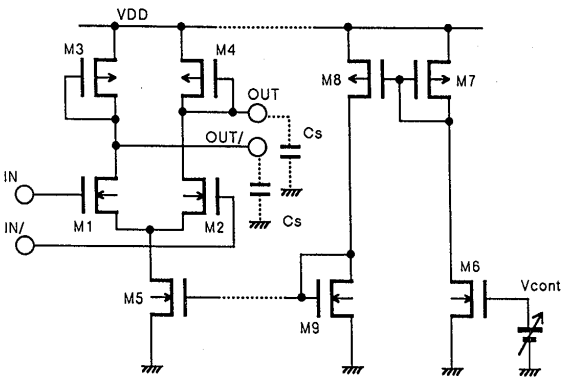
$$I_{cont} = (\beta_N/2) \cdot (V_{GS} - V_{th})^2 \tag{4}$$

where β_N is the transconductance parameter and V_{th} is the threshold voltage of an NMOS transistor, then the delay t_{dnew} of a cell, which is calculated by using Eq. (1), becomes,

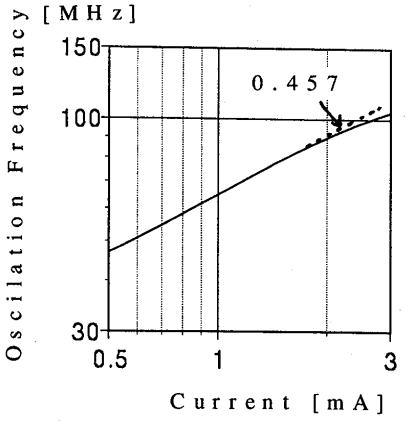
$$t_{dnew} = [1/\{\sqrt{\beta_N \beta_P} \cdot (V_{GS} - V_{th})\}] C_s \ln 2 \tag{5}$$



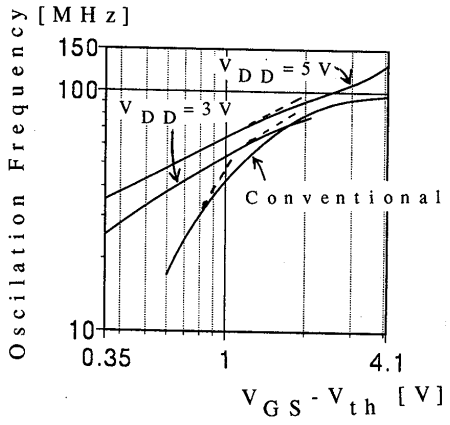
(a) Load replacement.



(b) A new delay cell circuit.



(c) The VCO simulation result for load replacement.



(d) The VCO simulation result for the circuit in Fig. 3(b).

Fig. 3 A new delay cell and VCO characteristics.

Now the frequency change controlled by the gate to source voltage V_{GS} of the NMOS transistor becomes linear.

The whole schematic of a new delay cell is shown in Fig. 3(b). The control circuit for the current is modified so that the current source transistor can not enter the linear region for the wide range of the control voltage.

5. Simulation Results

The performance of a new VCO circuit has been simulated by SPICE. The VCO consists of 15 stages of basic delay cells connected in series. Device parameters used are based on a 1.2 μm CMOS process. The circuit in Fig. 2(a), whose load resistors are replaced by transistors as shown in Fig. 3(a), is first simulated. Figure 3(c) shows the result. The slope of the curve is expected to be 1/2 and it is actually 0.457. The simulation result of the circuit in Fig. 3(b) is shown in Fig. 3(d). From the above discussion, the oscillation frequency should be proportional to $V_{GS}-V_{th}$. V_{th} is 0.9V in this case. The circuit performance with a 3 V power supply was also simulated and is plotted in Fig. 3(d). Curves show the improvement of linearity compared with one of the conventional circuits. However, the slopes obtained are 0.59 and 0.79 with 5 V and 3 V power supply, respectively. Curves can not follow the straight line when $V_{GS}-V_{th}$ becomes high because of the substantial logic delay of the delay cell. The duty cycle was verified to be exactly 50% by simulation although waveforms are not shown in figures. The reason why the curves in Fig. 3(d) do not have slopes close to 1 will be the subject of a future investigation.

6. Conclusion

A new VCO circuit with a differential type delay cell is proposed. It is seen by simulation that a new circuit has improved linearity compared with one of the conventional circuits. Further study is necessary however, because there still remains an unknown factor of the slope value.

References

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[2] Young, I. A., Greason, J. K. and Wong, K. L., "A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors," *IEEE J. Solid-State Circuits*, vol. 27, no. 11, pp. 1599–1607, Nov. 1992.