A Single-Power-Supply 10-b Video BiCMOS Sample-and-Hold IC

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Abstract—**A +5-V single-power-supply 10-b video BiCMOS sample-and-hold IC is described. Video speed, low power, and 10-b accuracy sample-and-hold operation has been achieved using a complementary connected buffer format sample switch. A high-speed p-n-p transistor used in the sample switch is formed by a combination of n-p-n and PMOS transistors. The sample-and-hold operation is accomplished by feeding back the hold capacitor voltage to the sample switch inputs, so that the inputs transfer symmetrically for the hold capacitor voltage at any input level. The sample-and-hold IC has been implemented in 1.2-μm BiCMOS technology and evaluated. The following results have been obtained: 185-MHz 3-dB bandwidth at 22-pF hold capacitor, 63-dB signal-to-noise ratio at 8-MHz full-scale input, 20-ns acquisition time at 1-V step input, 15-ns switching settling time, and 0.1% linearity error. Power dissipation is 150 mW.**

I. INTRODUCTION

THE DEMAND for a high-resolution video A/D converter has been increasing. A two-step parallel conversion scheme is most effective from the A/D converter power dissipation and cost viewpoints. In this case, however, a high-accuracy and low-power sample-and-hold circuit, operating at video frequency and above, is required as a pre-circuit for the A/D converter. Considering a future one-chip system containing the A/D converter, +5-V single power supply operation is also required for the sample-and-hold circuit. So far, several monolithic high-accuracy video sample-and-hold IC's have been developed [1]–[3]. However, they have used a comparatively large amount of power because a hold capacitor has been driven by a current source in them. Also, they all have needed two power supplies to maintain the 2-$V_{p\text{-}p}$ input full-scale range and to obtain high-accuracy characteristic. Previously, the authors developed a bipolar sample-and-hold IC using a complementary connected buffer as the sample switch to reduce power dissipation [4]. As a result, 10-b accuracy and a 20-MHz maximum conversion rate have been obtained at 400-mW power dissipation. However, the sample-and-hold IC also needed two power supplies and used high-speed p-n-p transistors. A p-n-p transistor, made by a standard process, has poor frequency performance, making video signals difficult to handle. This paper describes a single-power-supply 10-b video sample-and-hold IC, using 1.2-μm BiCMOS technology, that utilizes equivalent high-speed p-n-p transistors formed by a combination of n-p-n and PMOS transistors [5].

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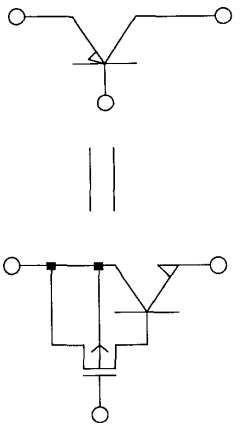

Fig. 1. Basic equivalent high-speed p-n-p transistor configuration.

II. EQUIVALENT HIGH-SPEED P-N-P TRANSISTOR REALIZATION

The authors proposed a sample-and-hold circuit that utilized a complementary connected buffer sample switch formed by an n-p-n and a p-n-p transistor, and obtained 10-b accuracy and a 20-MHz maximum conversion rate [4]. As a large output dynamic range can be obtained according to the circuit configuration, it is advantageous for single-power-supply operation. In BiCMOS technology, which is applicable for a one-chip system realization, however, it is difficult to supply a high-speed p-n-p transistor. So, the authors considered an equivalent high-speed p-n-p transistor, shown in Fig. 1. The equivalent high-

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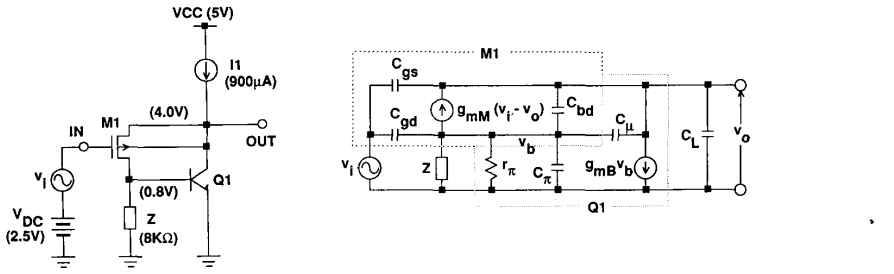


Fig. 2. Emitter-follower circuit, using the equivalent high-speed p-n-p transistor. (a) Circuit configuration. (b) Small-signal equivalent circuits.

TABLE I
n-p-n BIPOLAR TRANSISTOR PARAMETERS IN 1.2-μm BiCMOS PROCESS

Parameter	Symbol	Measured Value
Forward DC Current Gain	h_{fe}	89.2
Transconductance	g_{mB}	28.9 mS
Input Resistance	r_π	2.87 kΩ
Diffusion Capacitance	C_d	736 fF
Base-Emitter Junction Capacitance	C_{be}	66.3 fF
Base-Collector Junction Capacitance	C_μ	11.1 fF
Collector-Substrate Junction Capacitance	C_{cs}	75 fF
Base Transit Time	τ_F	25.5 ps
Base-Emitter Input Capacitance	C_π	802 fF
$C_\pi = C_d + C_{be}$, $C_d = \tau_F \times g_{mB}$		

TABLE II
PMOS TRANSISTOR PARAMETERS IN 1.2-μm BiCMOS PROCESS

Parameter	Symbol	Measured Value
Transconductance	g_{mM}	0.60 mS
Drain-Bulk Junction Capacitance	C_{db}	192 fF
Gate-Channel Capacitance	C'_{gs}	93.5 fF
Gate-Source Overlap Capacitance	C_{gsovl}	8 fF
Gate-Drain Overlap Capacitance	C_{gdovl}	8 fF
Bulk-Substrate Junction Capacitance	C_{bss}	224 fF
$C_{gs} \cong C'_{gs} + C_{gsovl}$		

speed p-n-p transistor is formed by the combination of an n-p-n and a PMOS transistor. As the gate–source voltage for the PMOS transistor can be set to about -1 V under actual operating conditions, the circuit shown in Fig. 1 is equivalent to a p-n-p transistor with -1-V base–emitter voltage.

It is very important to analyze the equivalent high-speed p-n-p transistor because the p-n-p transistor performances decide the characteristics for the sample-and-hold circuit, for example, acquisition time, distortion level, etc. As the equivalent p-n-p transistor is actually used in the emitter-follower circuit configuration, the authors have analyzed the circuit shown in Fig. 2(a). DC current flow in the PMOS $M1$ is controlled by an impedance Z to improve frequency response. The simplified small-signal equivalent circuit for Fig. 2(a) is shown in Fig. 2(b). Parameter meanings are as follows:

v_i input signal,
C_{gs}, C_{gd}, C_{db} PMOS $M1$ gate–source, gate–drain, and drain–bulk capacitances,
g_{mM} PMOS $M1$ transconductance,
r_π n-p-n $Q1$ base–emitter resistance,
C_π, C_μ n-p-n $Q1$ base–emitter and base–collector capacitances,
g_{mB} n-p-n $Q1$ transconductance,
C_L $M1$ bulk–substrate capacitance (C_{bss})+ $Q1$ collector–substrate capacitance (C_{cs}).

In the actual calculation, the 1.2-μm BiCMOS process device parameters have been used, considering IC implementation. The analyzed operating point is also shown in Fig. 2(a). The $M1$ channel length and width are 1.2 and 90 μm, respectively. The $Q1$ emitter size is 3×5 μm^2. Device parameter values are shown in Tables I and II.

The small-signal analysis results are discussed next.

A. Output Impedance Z_o

As indicated in Fig. 2(b), the output impedance in the low-frequency region is obtained as

$$Z_o = \frac{v_o}{i_o} = \frac{1}{g_{mM}[1 + g_{mB}(Z // r_\pi)]}. \quad (1)$$

As $Z \gg r_\pi$ and $h_{fe} \gg 1$,

$$Z_o \sim \frac{1}{g_{mM} \cdot h_{fe}}. \tag{2}$$

This shows that the output impedance shown in Fig. 2(a) is reduced by $1/h_{fe}$ of that for the source-follower circuit, using PMOS $M1$. Using the values shown in Tables I and II, $Z_o = 18.7\ \Omega$ is calculated. This value is comparable to that for a p-n-p emitter-follower circuit.

B. Voltage Gain G(s)

From Fig. 2(b),

$$G(s) = \frac{v_o(s)}{v_i(s)} = \frac{a_0 + b_1 \cdot s + b_2 \cdot s^2}{a_0 + a_1 \cdot s + a_2 \cdot s^2} \tag{3}$$

$$a_0 = g_{mM} \cdot g_{mB} \tag{4}$$

$$a_1 = g_{mM} \cdot (C_\pi + C_{gd}) + g_{mB} \cdot (C_\mu + C_{bd} + C_{gs}/h_{fe} + C_L/h_{fe}) \tag{5}$$

$$a_2 = (C_\mu + C_{bd}) \cdot (C_\pi + C_{gd}) + (C_{gs} + C_L) \cdot (C_\pi + C_\mu + C_{bd} + C_{gd}) \tag{6}$$

$$b_1 = g_{mM} \cdot (C_\pi + C_{gd}) + g_{mB} \cdot (C_{gs}/h_{fe} - C_{gd}) \tag{7}$$

$$b_2 = C_{gd} \cdot (C_\mu + C_{bd}) + C_{gs} \cdot (C_\pi + C_\mu + C_{bd} + C_{gd}) \tag{8}$$

are obtained as $Z \gg r_\pi$ and $h_{fe} \gg 1$.

In the low-frequency region, from (3),

$$G(0) = \frac{a_0}{a_0} = 1 \tag{9}$$

is obtained. This indicates the emitter-follower operation.

For higher frequency, the authors have attempted to simplify (3) using the values shown in Tables I and II. Then, below about 700 MHz, (3) is approximated as

$$G(s) \sim \frac{a_0}{a_0 + a_1 \cdot s}. \tag{10}$$

From this equation, the 3-dB bandwidth for the emitter-follower circuit is obtained as

$$f_{-3\,\mathrm{dB}} = \frac{a_0}{2 \cdot \pi \cdot a_1} = \frac{g_{mM} \cdot g_{mB}}{2 \cdot \pi \cdot \left[g_{mM} \cdot (C_\pi + C_{gd}) + g_{mB} \cdot (C_\mu + C_{bd} + C_{gs}/h_{fe} + C_L/h_{fe}) \right]} \sim \frac{g_{mM} \cdot g_{mB}}{2 \cdot \pi \cdot (g_{mM} \cdot C_\pi + g_{mB} \cdot C_{bd})}. \tag{11}$$

Fig. 3 shows the results calculated using (3) and (10), and the SPICE simulation result. From these results, the 470-MHz 3-dB bandwidth is obtained. This value is approximately consistent with that calculated from (11), which is 458 MHz.

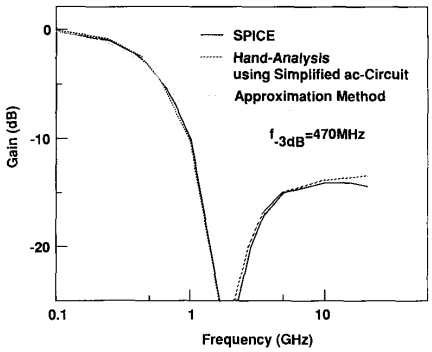


Fig. 3. Emitter-follower circuit frequency responses, using the equivalent high-speed p-n-p transistor.

Equation (11) shows that the 3-dB bandwidth is mainly decided by g_{mM} and C_{bd} for PMOS $M1$ in the 1.2-μm BiCMOS process, because $g_{mB} \cdot C_{bd}$ is dominant in the denominator in (11), and it is necessary to increase g_{mM} and to decrease C_{bd} in order to increase $f_{-3\mathrm{dB}}$. It is considered that the device miniaturization is effective for that. Using 0.8-μm BiCMOS technology, $f_{-3\mathrm{dB}}$ increases to about 1.5 GHz, because g_{mM} increases to 1.5 times and C_{bd} decreases to 0.45 times. A p-n-p transistor, with gigahertz bandwidth, may be realized by the configuration shown in Fig. 1.

III. Sample-and-Hold Circuit Design

The authors have designed a +5-V single-power-supply sample-and-hold circuit using the equivalent p-n-p transistor shown in Fig. 1. A schematic of the BiCMOS sample-and-hold circuit is shown in Fig. 4. The circuit is based on the one in [4] and consists of a complementary connected buffer format sample switch, a hold capacitor C_h, and buffer circuits to feed back the hold capacitor voltage V_{Ch} to the sample switch in the holding mode. The equivalent high-speed p-n-p transistors are used in the input stage and output stage for the sample switch and the feedback buffer circuits. In order to suppress the V_{GS} variation for PMOS transistors $M2$, $M6$, and $M11$ due to the input (V_{IN}) level, cascode-connected PMOS transistors ($M3$, $M7$, and $M12$) are used instead of $M1$

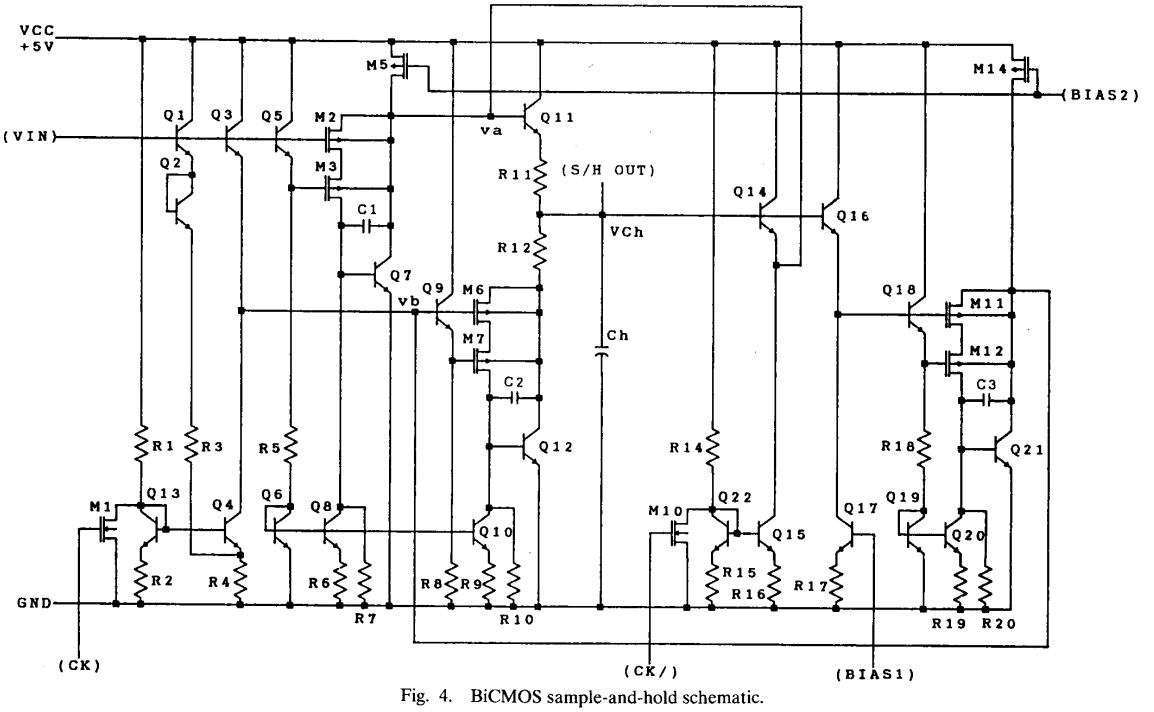


Fig. 4. BiCMOS sample-and-hold schematic.

in Fig. 2, and a parallel-connected resistor and voltage-to-current amplifier are used as impedance Z in Fig. 2. PMOS $M6$ dimensions are $W/L = 120\ \mu m/1.2\ \mu m$ to reduce the output impedance in the sample switch. Idling current for the output stage is 1.4 mA. Capacitors $C1$, $C2$, and $C3$ are used to reduce ringing voltage in the sample-and-hold operation.

The sampling mode and the holding mode are explained using Figs. 5 and 6. Fig. 5 shows the transition waveforms from the holding to the sampling mode and the equivalent circuit in the sampling mode. v_a and v_b are the base voltages for n-p-n $Q11$ and n-p-n $Q9$, respectively. v_a and v_b, which are held symmetrically for V_{Ch} in the holding mode as described later, rise up to $V_{IN} - V_{GSM2}$ due to $M2$ activation, and go down to $V_{IN} - V_{BEQ3}$ due to $Q3$ activation. Then, $Q11$ and the equivalent p-n-p transistor, formed by $M6$ and $Q12$, construct a complementary connected buffer, as shown in Fig. 5(b). Hold capacitor C_h is charged by the emitter-follower circuit for $Q11$ or discharged by the emitter-follower circuit for the equivalent p-n-p transistor. It is predicted that a small acquisition time will be obtained by the broad bandwidth and the small output impedance for the sample switch. According to SPICE simulation, a 15.5-ns acquisition time at a 1-V step, a 244-V/μs rising slew rate, and a 300-V/μs falling slew rate have been obtained.

The transition waveforms from the sampling to the holding mode, and the equivalent circuit in the holding mode are shown in Fig. 6. In the holding mode, v_a and v_b are transferred to $V_{Ch} - V_{BEQ14}$ and $V_{Ch} - V_{BEQ16} - V_{GSM11}$

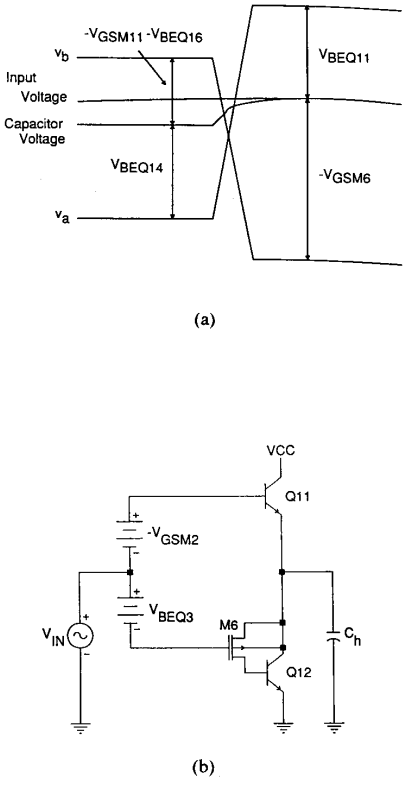


Fig. 5. (a) Waveform and (b) equivalent circuit in the sampling mode.

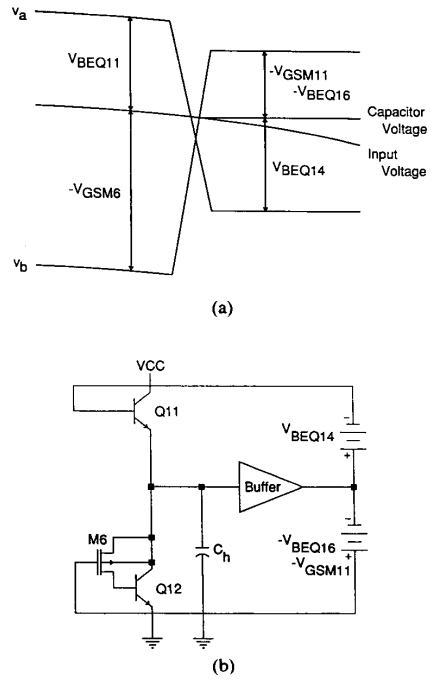


Fig. 6. (a) Waveform and (b) equivalent circuit in the holding mode.

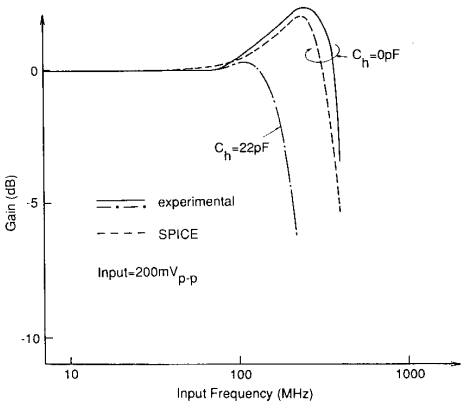
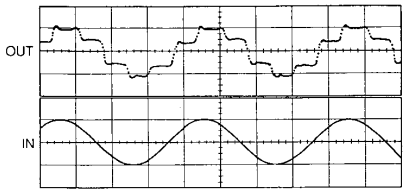


Fig. 7. Frequency responses in the sampling mode.



Sampling Rate : 30MHz, Input Frequency : 5MHz.
Vertical : 500mV/div., Horizontal : 50ns/div.

Fig. 8. Typical input and output waveforms for the sample-and-hold.

by activating the feedback buffer circuits, respectively. The $Q11$ base–emiter voltage and the $M6$ gate–source voltage are reverse biased at $-V_{BEQ14}$ and $-V_{BEQ16}-V_{GSM11}$, respectively. As a result, $Q11$, $M6$, and $Q12$ are cut off and V_{Ch} is held. It is seen from the transition waveforms that V_{BEQ11} and V_{GSM6} are always biased, under the same conditions, both in the sampling and in the holding mode. For this reason, the current injected to C_h and the current extracted from C_h are constant, and the distortion due to charge offset is suppressed. By tuning the $Q11$ and $M6$ dimensions, pedestal offset is also decreased. Additionally, as the $Q11$ base and the $M6$ gate are kept in a low-impedance condition by the feedback buffer circuits in the holding mode, the hold-mode feedthrough is suppressed. According to SPICE simulation, a 7-ns switching settling time, a 21-mV pedestal offset, and a -79-dB hold-mode feedthrough at 10-MHz 1-V_{p-p} input have been obtained.

The full-scale input range has been set to 2 to 3 V (1 V_{p-p}). Then, the minimum voltage values for V_{DSM5}, V_{DSM4}, V_{CEQ4}, and V_{CEQ15} are, respectively, about -1, -1.3, 1.2, and 1.5 V. These values are sufficient for current-source operation, considering voltage supply variations.

IV. Experimental Results

The BiCMOS sample-and-hold IC has been fabricated in 1.2-μm BiCMOS technology with double metal layers and evaluated. An n-p-n transistor has an ion-implanted emitter with 3-μm stripe length. The maximum f_T, V_A, and I_K values are 6 GHz, 50 V, and 8 mA, respectively. The channel length and threshold voltage for the MOS transistor are 1.2 μm and 0.8 V, respectively. A poly-Si resistor can be utilized. A double-layer poly-Si capacitor can also be utilized, but it has not been used for this sample-and-hold IC. The IC has been evaluated using an external capacitor for the hold capacitor.

Fig. 7 shows the frequency responses in the sampling mode. These responses have been measured at $C_h = 0$ and 22 pF. The input amplitude is about 200 mV_{p-p} in the 50-Ω termination condition. The SPICE simulation result at $C_h = 0$ pF is also shown for comparison. A 400-MHz 3-dB bandwidth has been obtained at $C_h =$ 0 pF. It is considered that the peak around 250 MHz results from the stray capacitance connected to the emitter for the equivalent p-n-p transistors. The 3-dB bandwidth decreases to 185 MHz at $C_h = 22$ pF.

Fig. 8 shows typical input and output waveforms at $C_h = 22$ pF. The input frequency is 5 MHz and the sampling rate is 30 MHz. It is seen that the 1-V_{p-p} input signal is sampled and held for +5-V single power supply. The rising and falling slew rates are 242 and 276 V/μs, respectively.

Fig. 9 shows the input signal level signal-to-noise ratio (SNR) dependence at $C_h = 22$ pF. Bandwidth is 15 MHz. The full-scale input level is 1 V_{p-p}. The SNR at an

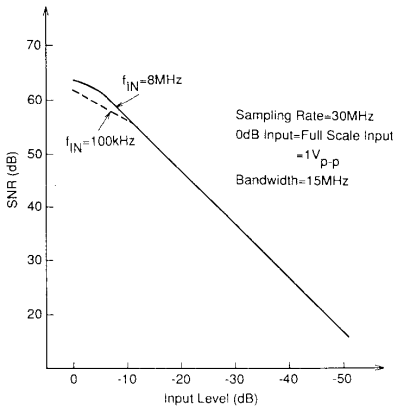


Fig. 9. Input signal level SNR dependences.

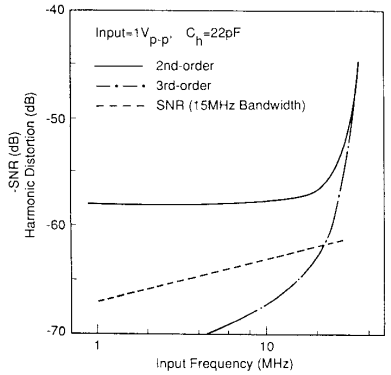


Fig. 10. Harmonic distortion and SNR frequency responses.

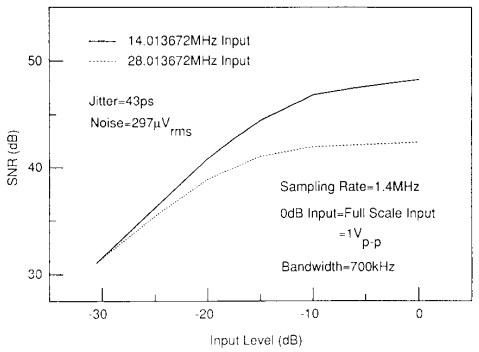
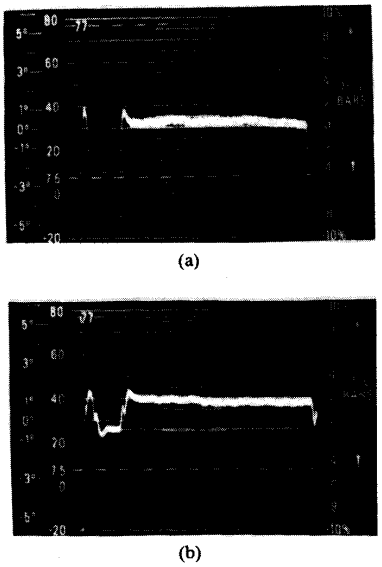


Fig. 11. Input signal level SNR dependences.



(a)

(b)

Fig. 12. (a) Differential gain (= 0.5%) and (b) differential phase (= 0.3°) at a 20-MHz sampling rate.

8-MHz input frequency is approximately equal to that at a 100-kHz input frequency. The SNR values at 8-MHz full scale and −20-dB inputs are 63.7 and 46.8 dB, respectively. The reason for SNR degradation at a 100-kHz input larger than −10 dB seems to be jitter in the input signal, but has not been clarified yet.

Fig. 10 shows the frequency responses for the harmonic distortion level in the sampling mode and SNR in the sample-and-hold operation. The second-order distortion is dominant and is −58 to −59 dB between 1 and 10 MHz. The SNR at 15-MHz bandwidth is larger than 62 dB below 10 MHz.

The aperture uncertainty evaluation refers to the method in [6]. The results obtained, using a 12-b ADC, are shown in Fig. 11. The sampling rate is 1.4 MHz and the input frequencies are 14.013672 and 28.013672 MHz. The hold capacitor value is 22 pF. From the results, 43-ps jitter and 297-μV_{rms} voltage noise have been calculated for the evaluated sampling system. As the 43-ps jitter contains the input signal jitter and the clock signal jitter, the aperture uncertainty for the sample-and-hold can be expected to be less than 43 ps.

The characteristics for differential gain and differential phase are important for TV signal processing. They are shown in Fig. 12(a) and (b). The differential gain is 0.5% and the differential phase is 0.3° at a 20-MHz sampling rate. The hold capacitor value is 22 pF.

TABLE III
MAIN SAMPLE-AND-HOLD CHARACTERISTICS

Input Range	1 V	Acquisition Time	20ns (1V step)
Supply Voltage	+ 5 V	Switching Settling Time	15 ns
Power Dissipation	150 mW	Aperture Uncertainty	< 43 ps
Linearity	0.1 %	Hold Mode Droop Rate	14 mV/μs
SNR	63 dB (15MHz bandwidth)	Hold Mode Feedthrough	- 62 dB (5MHz, 1Vp-p)
Differential Gain	0.5 %	Pedestal Offset	10 mV
Differential Phase	0.3 degree	Die Area	370 x 740 μm^2

The main BiCMOS sample-and-hold IC characteristics are listed in Table III. The acquisition time to 0.1% is 20 ns at 1-V step and the switching settling time to 0.1% is 15 ns. The hold-mode feedthrough is less than −60 dB at 1-V_{p-p} input below 10 MHz. The hold-mode droop rate is 14 mV/μs. The power dissipation is 150 mW. Fig.

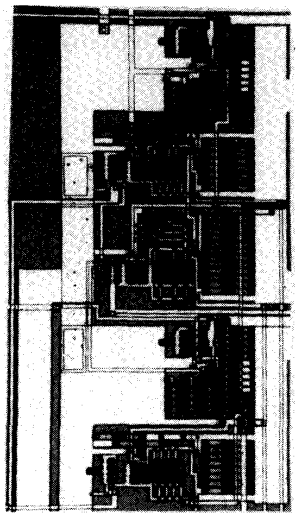


Fig. 13. Sample-and-hold microphotograph.

13 shows a microphotograph of the sample-and-hold circuit shown in Fig. 4. The chip area is 0.27 mm^2.

V. Conclusion

A +5-V single-power-supply BiCMOS sample-and-hold IC has been implemented in 1.2-μm BiCMOS technology and evaluated. It has been clarified that an equivalent p-n-p transistor, formed by the PMOS and n-p-n transistor combination, has a 3-dB bandwidth broader than 400 MHz. The BiCMOS sample-and-hold circuit, designed using the equivalent p-n-p transistors and the hold capacitor voltage feedback buffer circuits, has realized 10-b accuracy and video speed operation with +5-V single power supply. The power dissipation is only 150 mW.

Using this sample-and-hold IC and a two-step parallel format 10-b A/D converter, video signal 10-b A/D conversion is possible with +5-V single power supply and low power consumption. They are applicable to high-quality digital video equipment, such as high-definition TV.

Acknowledgment

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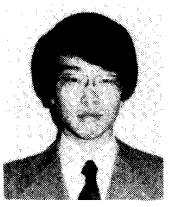

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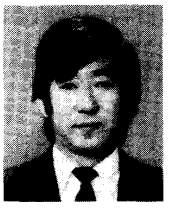
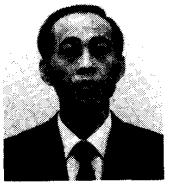
In 1984 he joined Toshiba Corporation. Since then he has been engaged in design of mixed analog and digital IC/LSI's using bipolar and BiCMOS technology.



Yasuhiro Sugimoto (M'76–S'79–M'80) received the B.S.E.E. degree in electrical engineering from the Tokyo Institute of Technology in 1973 and the M.S.E. degree in computer-aided design from the University of Michigan in 1980.

In 1973 he joined Toshiba Corporation. Since then he has been engaged in design of mixed analog and digital IC/LSI's. He is currently a senior specialist in the semiconductor division.

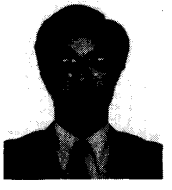
Mr. Sugimoto is a registered consulting engineer in electricity in Japan.



Makoto Noda received the B.S. and M.S. degrees in electronic engineering from Yamagata University in 1973 and 1975, respectively.

In 1975 he joined Toshiba Corporation. Since then he has been engaged in research and development design of microprocessors, digital signal processors, and BiCMOS LSI. He is now Manager of the Advanced Logic/Memory Technology Department, Semiconductor Device Engineering Laboratory.

Mr. Noda is a member of the Institute of Electronics, Information and Communication Engineers of Japan.



Takao Ito (S'86–M'87) received the B.E. degree from the University of Tokyo in 1979, and the M.Eng. degree in electrical engineering from Cornell University, Ithaca, NY, in 1987.

In 1979 he joined Toshiba Corporation, where he was engaged in the development of low-power and high-speed bipolar devices. Since 1988 he has been working in the field of BiCMOS LSI's.

Mr. Ito is a member of the Institute of Electronics, Information and Communication Engineers of Japan.

Yoshito Suwa received the B.S. degree in applied chemistry from Keio University, Tokyo, Japan, in 1985.

In 1985 he joined Toshiba Corporation. Since then he has been engaged in the development of bipolar and BiCMOS devices.