A 96 kHz 16 BIT DUAL CHANNEL A/D CONVERTER LSI FOR DIGITAL AUDIO APPLICATIONS

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ABSTRACT

A low cost 96 kHz 16 bit dual channel A/D converter LSI has been developed. Its S/N ratio is 93 dB and THD is 0.003%. Combining with anti-aliasing digital filter, we can reduce the order of analog filter proceding to A/D converter which might be harmful to the sound quality.

1. Introduction

Recently digital audio equipments have become very popular due to the development of semiconductor digital LSIs. In these equipments, such as digital audio tape (DAT), audio signal processor (ASP) and digital amplifier, high resolution and low cost A/D converter LSI is required as the key component.

Considering this situation, we have developed a low cost 96 kHz 16 bit dual channel A/D converter LSI for digital audio applications by using our conventional bipolar process of A-NSA.

This A/D converter LSI is a coarse-fine integration type. We have achieved high speed conversion (96 kHz, dual channel) by using new circuit technology.

So in combination with anti-aliasing digital filter we can reduce the order of analog filter preceding to A/D converter which might be harmful to the sound quality.

To realize low cost, this LSI is fabricated by our conventional bipolar process A-NSA(Advanced Nitride Self-Aligned Process).

2. Features of A-NSA

Features of A-NSA are mentioned as follows.

(1) High speed NPN Transistor (ft=2 GHz)

(2) High ft (500 MHz) Vertical PNP Transistor

(3) Poly-Silicon Resistor (low parasitic capacitance)

(4) High β NPN Transistor (β>500)

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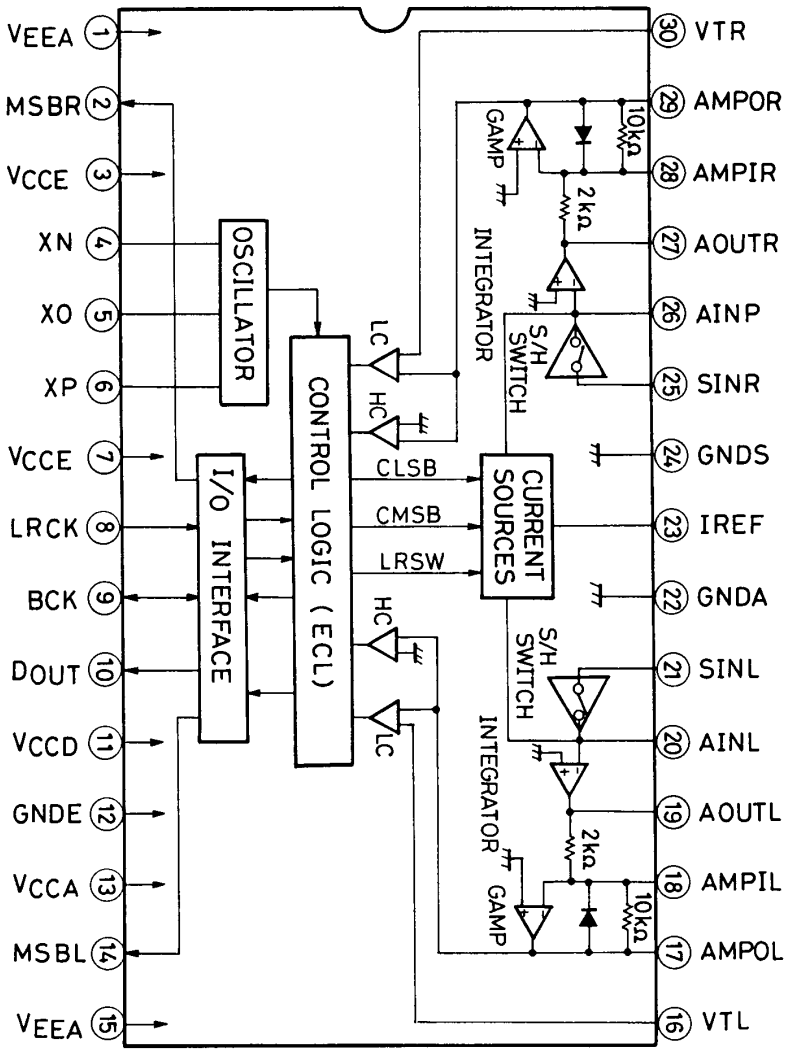

Fig. 1 BLOCK DIAGRAM

3. Block Diagram

Fig. 1 shows a block diagram of this LSI.

It consists of 9 blocks.

(1) Integrators

(2) S/H Switches

(3) Two Constant Current Sources (128:1)

(4) Gain Amplifiers (GAMP)

(5) Comparators H (corresponding to upper 8 bits)

(6) Comparators L (corresponding to lower 8 bits)

(7) Control Logics (ECL)

(8) I/O Interfaces

(9) Internal Oscillator

4. Principle of A/D Conversion

Fig. 2 shows the principle of A/D conversion. First switch (S1) is closed and (SM), (SL) is open, so input analog signal Vs is sampled into capacitor C. Secondly (S1), (SM) and (SL) are open respectively and charge of capacitor C is holded. Thirdly (S1) is open, (SM) is closed and (SL)is open, so charge of capacitor C is discharged until output voltage of GAIN AMP. crosses ground level (coarse integration). Finally (S1), (SM) is open and (SL) is closed, fine integration starts and continues until output voltage of GAIN AMP. crosses VT level. This A/D converter have 16 bit counter (8 bit + 8 bit) and coarse integration time and fine integration time are counted respectively by master clock.

5. Problem to Realize High Speed Conversion

IM:IL is determined to 128:1 from the limitation of transistor's ΔVBE and the deviation of the ratio of resistor value. (IM and IL are constant current sources shown in Fig. 2.) Then construction of 16 bit counter is (9 bit + 7 bit).

If we want to realize dual channel 16 bit A/D conversion of 96 kHz sampling frequency, master clock frequency: Fmck should be(considering VT margin)

$$Fmck=(512+64+2x128)x2x96kHz=160MHz$$

where 512 : 9 bit
64 : dummy counts which reduces transient current source non linearity
128 : 7 bit

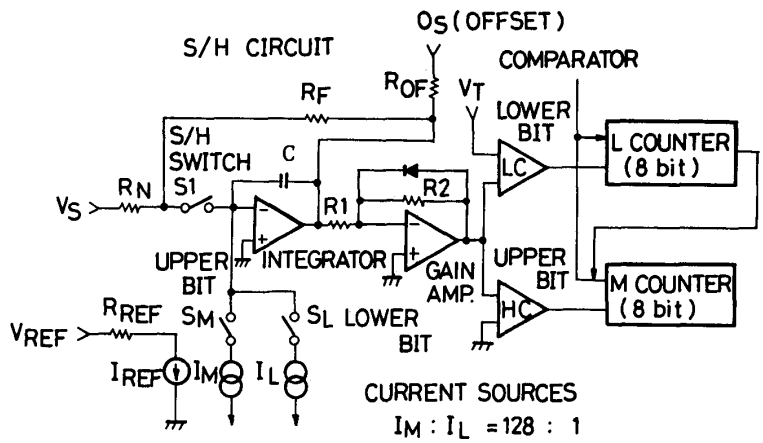

Fig. 2 A/D CONVERTER CONSTRUCTION

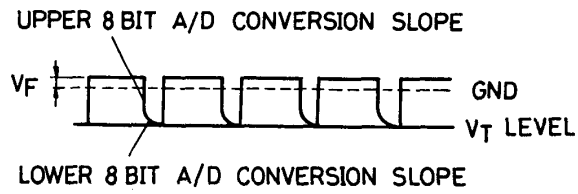

Fig. 3 GAIN AMP. OUTPUT WAVEFORM

It is very difficult for this type of A/D converter to make operate stably at this high frequency with low power consumption.

6. High Speed A/D Conversion

We have solved this problem by using new circuit technology.

Fig. 4 shows a new 8 bit counter which we used for the LSB counter. It is a part of control logic block in Fig. 1. In Fig. 4, when "STP" signal (current source stop signal) which is from LSB comparator is changed as a solid line in Fig. 4', turning point ta is t1<ta<t2, Q1 turns from "low" to "high" at t3 and Q2 turns from "low" to "high" at t2, so output of TFF (15) remains "low" state.

Next when "STP" signal is a broken line, turning point tb is t2<tb<t3, Q1 is same as a solid line and Q2 turns from "low" to "high" at t4, so output of AND GATE (25) DJ is a broken line. And output of TFF (15) turns "high" state.

Using this technology we can lower master clock frequency.

IM:IL is determined to 128:1 and construction of 16 bit counter is (8 bit + 7 bit + 1 bit). We use this technology for LSB counter.

Master clock frequency: Fmck becomes(considering VT margin)

$$Fmck=(256+64+2\times128)\times2 \times 96\ \text{kHz}=111\ \text{MHz}$$

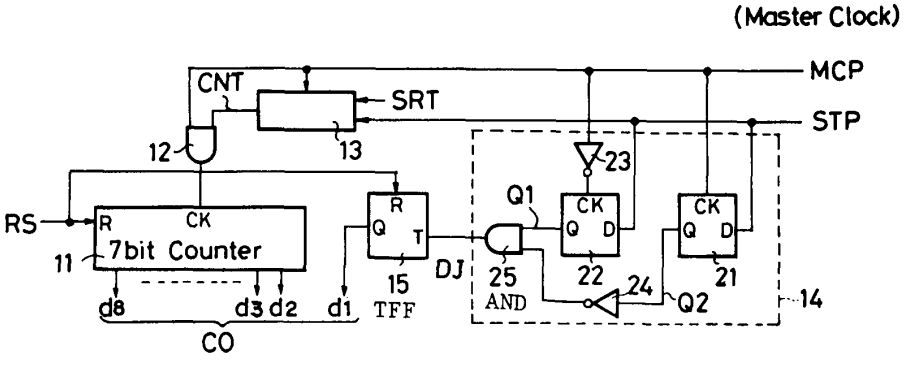

Fig. 4 NEW 8BIT COUNTER CIRCUIT

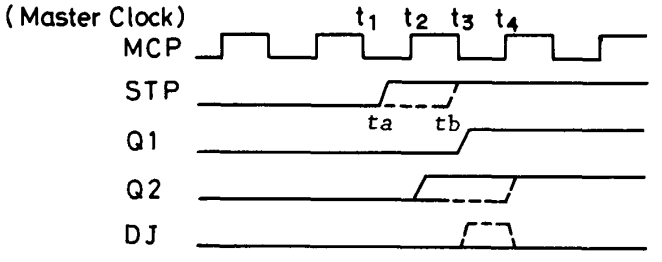

Fig. 4' TIMING CHART

where 256 : 8 bit
64 : dummy counts which reduces transient current source non linearity
128 : 7 bit

We could make this A/D converter LSI operate stably with low power consumption.

7. DC Offset Compensation Circuit

Another feature of this A/D converter LSI is that it includes DC offset compensation circuit. In Fig. 5 "MSB" terminal corresponds to "MSBR" and "MSBL" in Fig. 1(dual channel). Input voltage of "MSB" change high or low level in synchronous with sampling clock. If MSB of internal 16 bit data is "0", voltage of "MSB" terminal is +1 volt. Next when MSB is "1", voltage of "MSB" becomes to -1 volt.

DC offset compensation circuit is constructed being shown in Fig. 5. If "MSB" terminal is +1 volt, output voltage of GAIN AMP. rises and digital data increases. When "MSB" is -1 volt, voltage of GAIN AMP. falls and digital data decreases.

In this way DC offset compensation circuit operates well.

Fig. 6 shows an output stage circuit of "MSB".

When MSBI is high level and MSBI/ is low level, base voltage level of Q5 is higher than that of Q6. Then Q5 becomes cutoff state and Q6 becomes on state. So I3(200μA) flows from R3(5 kΩ) to GND and voltage of MSBO becomes +1 volt. Next when MSBI is lower than MSBI/, Q5 becomes on state. So I3(200μA) flows from Q5 to Q7. Q7 and Q8 are current mirror circuit and current(200μA) from GND to MSBO through R3(5 kΩ). Then voltage of MSBO becomes -1 volt.

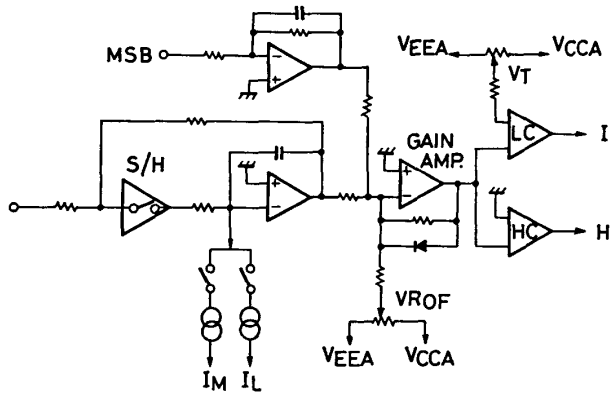

Fig. 5 DC OFFSET COMPENSATION CIRCUIT

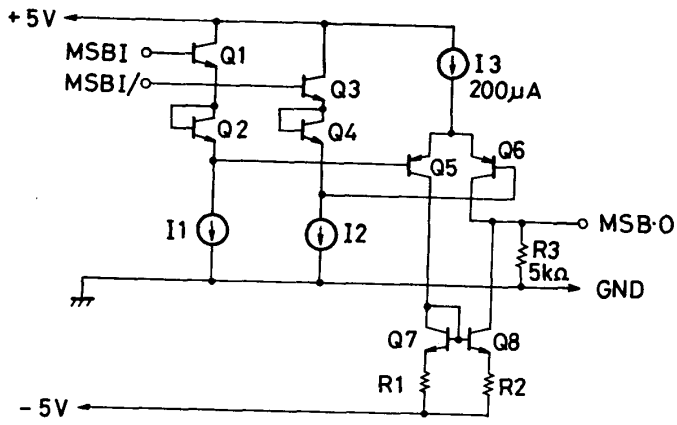

Fig. 6 MSB OUTPUT STAGE

8. Performance of A/D Converter LSI

Fig. 7 shows the frequency characteristics of THD. THD is about 0.003% at 1 kHz (Full Scale Input). The S/N ratio is 93 dB. Table 1 shows the performance of this LSI.

9. Conclusion

A 96 kHz 16 bit dual channel A/D converter LSI has been developed. It has realized low cost and has sufficient performance for digital audio applications.

This A/D converter LSI will be used in various digital audio equipments in combination with anti-aliasing digital filter.

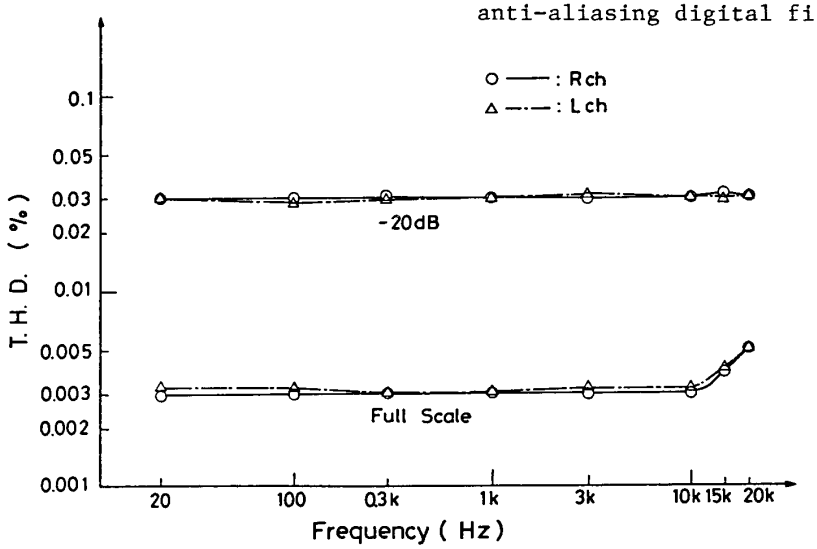

Fig. 7 T.H.D. vs. Frequency of A/D Converter LSI

Resolution	16 bits
Sampling Frequency	96 kHz
Master Clock Frequency	123 MHz
S/N	93 dB (with A weight)
THD	0.003 % (Full Scale)
Input Channel	L, R 2 Channel
Supply Voltage	± 5 V
Power Consumption	600 mW
Chip Size	4.19 mm x 3.90 mm
Number of Elements	3000
Fabrication Technology	2μm Bipolar (A·NSA)

Table 1 PERFORMANCE OF A/D CONVERTER LSI

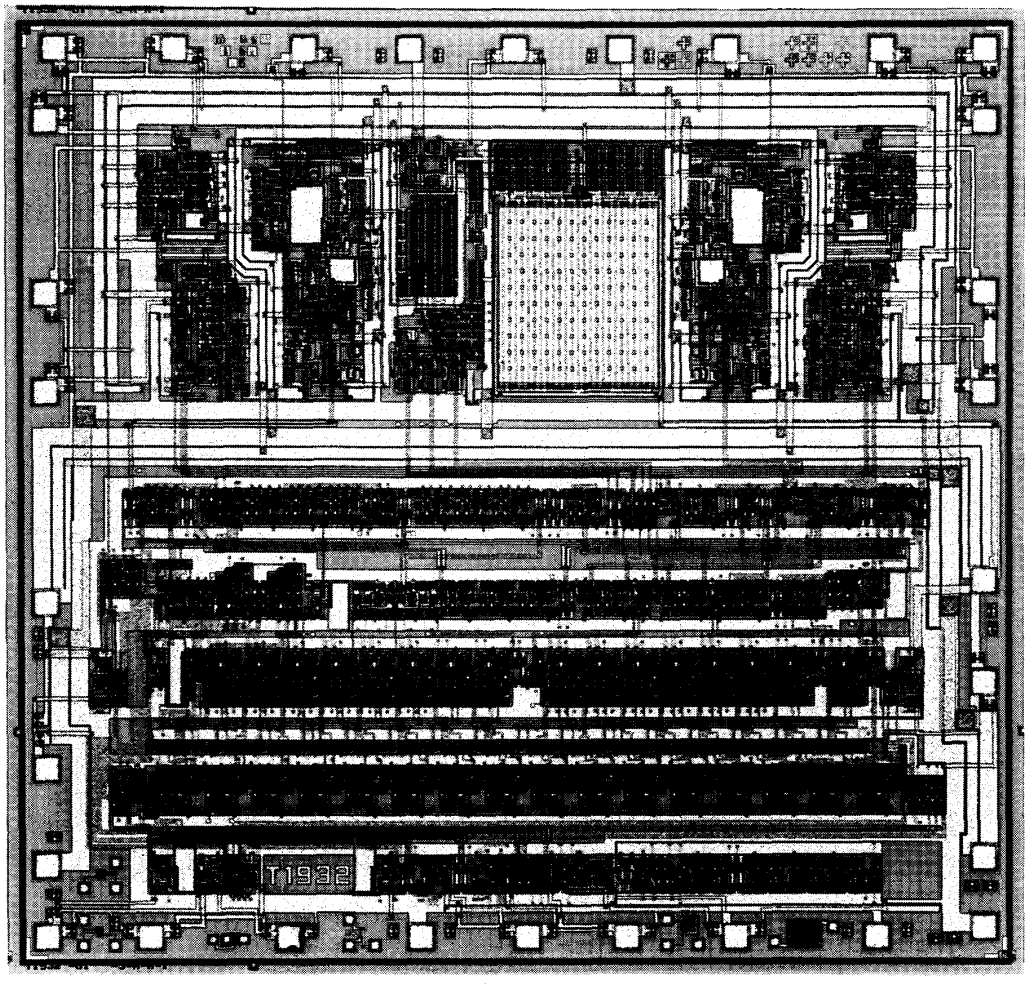

Fig. 8 Microphotograph of A/D Converter LSI

10. Acknowledgements

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11. Reference

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12. Biographies

Michinori Nakamura was born in Okayama, Japan, on May 22, 1955. He received the B.S. degree in electrical engineering from the University of Tokyo, Tokyo, Japan in 1978.

He joined Toshiba Corporation, Kawasaki, Japan, in 1978, and has been engaged in design and development of high-speed and high-accuracy Bipolar devices.

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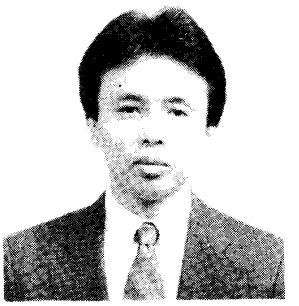

Yukio Hasegawa was born in Fukui, Japan, on May 6, 1955. He received the B.S. degree in electrical engineering from Fukui Technical College, Fukui, Japan in 1976.

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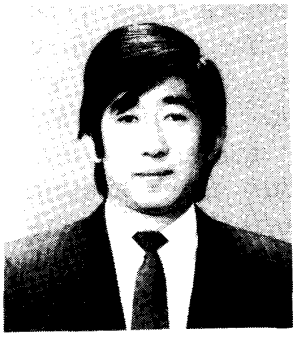

Yasuhiro Sugimoto received the B.S.E.E. in electrical engineering from the Tokyo Institute of Technology, Tokyo, Japan in 1973, and the M.S.E. in computer aided design from the University of Michigan, Ann Arbor, Michigan in 1980.

In 1973 he joined Toshiba Corporation where he has been involved in the development of new technologies for analog integrated circuits.

During 1979 — 1980 he was on leave at the University of Michigan, Ann Arbor, Michigan, where he worked on the computer aided circuit design for integrated circuits.

Mr. Sugimoto is a member of the Institute of Electronics, Information and Communication Engineers of Japan.