A Near 1-V Operational, 0.18-μm CMOS Passive Sigma-Delta Modulator with 77 dB of Dynamic Range

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SUMMARY A low-voltage operational capability near 1 V along with low noise and distortion characteristics have been realized in a passive sigma-delta modulator. To achieve low-voltage operation, the dc voltage in signal paths in the switched-capacitor-filter section was set to be 0.2 V so that sufficient gate-to-source voltages were obtained for metal-oxide-semiconductor (MOS) switches in signal paths without using a gate-voltage boosting technique. In addition, the input switch that connects the input signal from the outside to the inside of an integrated circuit chip was replaced by a passive resistor to eliminate a floating switch, and gain coefficients in the feedback and input paths were modified so that the bias voltage of the digital-to-analog converter could be set to $V_{DD}$ and 0 V to easily activate MOS switches. As the signal swing becomes small under low-voltage operational circumstances, correlated double sampling was used to suppress the offset voltage and the 1/f noise that appeared at the input of a comparator. The modulator was fabricated using a standard CMOS 0.18-μm process, and the measured results show that the modulator realized 77 dB of dynamic range for 40 kHz of signal bandwidth with a 40 MHz sampling rate while dissipating 2 mW from a 1.1 V supply voltage.

Key words: passive sigma delta, low voltage, switched capacitor filter, correlated double sampling

1. Introduction

According to the technology forecast, the supply voltage becomes less than 1.0 V in a 32-nm CMOS process [1]. This means that analog circuits have to operate under a 1 V supply voltage in the near future. However, it is extremely difficult to achieve high performance in analog circuits with this low supply voltage.

As the passive sigma-delta modulator (PSDM) [2]–[6] does not require precise analog circuits such as operational amplifiers or operational transconductance amplifiers, it is likely a candidate for use in future analog circuits. While a previous study [3] realized 1.5 V operation by using a 0.13-μm CMOS process, further reduction of the supply voltage is difficult because of problems such as the floating state in switches [7], the decrease of the signal-to-noise-and-distortion ratio (SNDR) due to the offset voltage in differential signal paths and the 1/f noise at the input of a comparator. A hybrid-type combined structure of active and passive filters has been proposed [8] to solve the SNDR issue.

However, the supply voltage for this structure is still 1.5 V and it involves the use of analog circuits.

In this work, we clarify the obstacles and limitations to achieving near-1 V operation of a PSDM. We then propose circuits that solve the above issues in order to realize near-1 V operation. The paper is organized as follows. In Sect. 2, obstacles to achieving low-voltage operation, namely the floating switch and small comparator input signal problems, are discussed. Section 3 shows how we eliminate the floating switches problem, and Sect. 4 describes how the small-signal problem at the input of the comparator is solved. Each proposed circuit is designed assuming a 1.0 V supply voltage. Section 5 shows chip evaluation results that verify the usefulness of the proposed circuits under a 1.1 V supply voltage. Section 6 concludes the study. The target specification of the supply voltage was 1.0 V for GSM etc, although the measurement results were under 1.1 V.

2. Obstacles to Achieve Low-voltage Operation

2.1 The Floating Switch

The floating switch problem is a primary concern in the design of low-voltage-switched capacitor circuits. To reduce the signal-dependent on-resistance of the switch, both n-type MOS (NMOS) and p-type MOS (PMOS) transistors are used to form a CMOS transmission gate.

Figure 1 shows the simulated on-resistance of a CMOS transmission gate driven by a 1.0 V driving signal. The switch on-resistance is determined by the overdrive voltage of the switching transistor. In this simulation, the size of the transistor in a CMOS switch were chosen to be 32 μm/0.18 μm (W/L) for NMOS and 64 μm/0.18 μm (W/L) for PMOS. The
on-resistance of a CMOS switch becomes extremely high when the signal input voltage is in the mid-range; we call a switch in such a state a “floating switch.” Floating switches directly affect the performance of the switched capacitor filter by, for example, causing distortion. Of course, the gate voltage could easily be boosted to strongly activate a NMOS transistor [9]; however, this is no longer the case, as the gate voltage cannot be boosted due to the reliability concern of the scaled CMOS process. The maximum gate voltage for a MOS switch should be limited to $V_{DD}$. In order to prevent the switch from entering the floating condition, we propose the use of the MOS switch in the region of the solid bold line where the switch has low on-resistance as shown in Fig. 1.

For switches used in the digital-to-analog converter (DAC) in the feedback path, two constant voltages that fix the signal dynamic range are required. We even scaled these two voltages to be $V_{DD}$ and 0 V so that the switch can be used in the states denoted by black circle points in Fig. 1.

### 2.2 Signal Level Becomes Very Small at the Input of the Comparator

Figure 2 shows the block diagram of the PSDM. In this system, the only active element is a comparator. $E_q$ stands for the quantization noise, $G$ for the comparator gain, $E_{com}$ for transistor noises at the comparator input and $H$ for the transfer function of the filter. The transfer function of the PSDM is given by the following equation.

$$ Y = X + \frac{E_q}{GH} + \frac{E_{com}}{H} $$

Equation (1) indicates that the influence of the comparator input noise $E_{com}$ on the output $Y$ is large because the loop filter $H$ does not have a gain, while the influence of the quantization noise $E_q$ is suppressed by a large comparator gain $G$.

The filter used in Chen’s PSDM [3] had a transfer function with 2 poles and 1 zero, which has no active elements. Figure 3 shows the filter frequency characteristics with 2 poles and 1 zero, where the clock frequency $f_s$ is assumed to be 100 MHz. The filter has no dc gain, and the signal is attenuated by 83 dB at half the clock frequency ($f_s/2$). As the input signal is modulated to around $f_s/2$ by comparison with the PWM feedback pulses, the signal components around $f_s/2$ suffer from a large attenuation by the filter and become very small at the input of the comparator. Moreover, the low-voltage operation means that the input signal amplitude is small, and therefore, the signal components around $f_s/2$ also become smaller than those seen in cases with a higher supply voltage. This creates a severe problem in obtaining a high SNDR at the input of the comparator.

### 3. Elimination of Floating Switches

#### 3.1 Floating Switches in the Switched Capacitor Filter

Figure 4 shows the second-order passive filter of a PSDM in which the switched capacitor circuit technique is used without an operational amplifier [3]. Each part in the dashed-line box acts as a resistor and realizes the second-order filter as a whole. All switches are CMOS switches and the symbols shown in reverse triangular shape are the bias voltage. In Fig. 4, voltages at the in and out terminals are commonly chosen to be half the supply voltage, that is, $V_{DD}/2$, because the feedback DAC in PSDM swings from $V_{DD}$ to ground. This means that the voltage at the in and out terminals becomes 0.5 V when $V_{DD}$ is 1 V. At that point it is very difficult for a CMOS switch to become turn-on in a low on-resistance environment with 0.5 V or less of gate-to-source voltage.

Figure 5 shows the input part of Fig. 4 with subfigures each of which shows the operating range for a switch accompanying word such as ‘NMOS ON’ or ‘PMOS ON.’ The switches surrounded by boxes are floating switches. Here $\phi_1$ and $\phi_2$ are non-overlap clocks. At $\phi_2$, the input signal is stored in the capacitor $C_{r1a}$, while the capacitor $C_{r1b}$ is dis-
charged. Then at $\phi 1$, the charge stored in cr1a is transferred to cr1b. In this design, the relationship among voltages at terminals ‘$V_a$’, ‘$V_{in}$’ and ‘$V_{bias}$’ becomes

$$V_a = V_{bias} - \frac{cr1a}{cr1a + cr1b} (V_{in} - V_{bias})$$

(2)

As both $V_{in}$ and $V_{bias}$ are chosen to be 0.5 V, the voltage at $V_a$ becomes 0.5 V. This means that the gate-to-source voltage $V_{gs}$ of a switch is only 0.5 V.

In order to avoid producing floating switches, $V_{bias}$ in Eq. (2) has been changed from 0.5 V to 0.3 V. $V_{bias}$ remains 0.5 V, and cr1a is cr1b. As a result, the voltage $V_a$ becomes 0.2 V as shown in Fig. 6.

By this modification, two floating switches are eliminated from Fig. 5 because the allowable gate bias voltage for a MOS transistor in a switch becomes 0.8 V. Also, the $V_{gs}$ of switches that are connected to the $V_{bias}$ node becomes 0.7 V. To maintain an easy interface with the outside signal of the integrated circuit, the input bias voltage $V_{in}$ remains $V_{DD}/2$.

The input switch is then replaced by a linear resistor to eliminate the third floating switch [10], as shown in Fig. 7. By these modifications, floating switches are eliminated from the switched capacitor filter.

3.2 The Floating Switch in the DAC

One floating switch remains in the feedback loop. Figure 8 shows the conventional DAC circuits. The voltages $V_{refp}$ and $V_{refm}$ are chosen such that $(V_{refp} - V_{bias})$ equals $(V_{bias} - V_{refm})$. $V_{refp}$ and $V_{refm}$ are 0.6 V and 0 V, respectively. However, this makes one of the DAC switches enter the floating state. Moreover, the reduction of the on-resistance of the DAC switches is the key to obtaining good modulator performance. Therefore, we took the black circle points in Fig. 1 for CMOS switches to be biased, and $V_{refp}$ and $V_{refm}$ were set to 1 V and 0 V, respectively, as shown in Fig. 9.

Scaling of signals is necessary to accommodate the new reference voltages $V_{refp}$ and $V_{refm}$ in the DAC. The gain scaling of the input signal $V_{in}$ and the feedback DAC output signal is shown in Fig. 10. By introducing scaling factors of $\alpha$ for the input signal $V_{in}$ and $\beta$ for the feedback DAC output signal, the voltage ‘$V_a$’ in Fig. 10 is calculated by the following equation.

$$V_a = \frac{cr1a}{cr1a + cr1b} (2 V_{bias} - V_{in}) + \frac{cr1b}{cr1a + cr1b} V_{refp,refm}$$

(3)

Where $V_a$ is the voltage swing at the summing node and $V_{refp,refm}$ is the voltage swing at the DAC output in Fig. 10. By substituting values of cr1a = 600 fF, cr1b = 200 fF, $V_{bias} = 0.3$ V and $V_{in} = 0.5$ V ± 80 mV, Eq. (3) becomes

$$V_a = -0.75 V_{in} + 0.45 + 0.25 V_{refp,refm}$$

(4)

In Fig. 10, the effective input signal at node ‘$V_a$’ is 0.12 V peak to peak (0.75 times the input signal), and the effective DAC output signal at node ‘$V_a$’ becomes 0.25 V.
peak to peak (0.25 times $V_{DD}$) centered at 0.2 V of dc voltage. By performing the scaling described above, the voltage of $V_{refp}$ in Fig. 9 can be 1 V, that of $V_{refm}$ can be 0 V, and $V_{refp}, refm$ becomes either 1 V or 0 V. Figure 11 shows the simulation results at the summing node Va using the Hspice simulation program. The DC signal level and the signal swing agreed well with the expected values. The maximum voltage is limited to 0.385 V, which ensures turn-on of a MOS switch under low resistance.

As a result, MOS switches that connect to $V_{refp}$ and $V_{refm}$ can be turned on easily because 1 V is used for the gate-to-source voltage of a switch transistor.

4. Avoiding the Influence of the Small Signal-Level at the Input of the Comparator

4.1 Effects of the Small Signal-Input-Voltage

Next, we will examine the other major problem, namely that the signal level becomes very small at the input of the comparator.

Figure 12 is the whole PSDM system and shows how the offset voltage $V_{off}$ at the input of the comparator produces an imbalance in the signal path voltages. The feedback and filter parts are differentially configured. When the offset voltage $V_{off}$ exists at the input of a comparator xcmp, as shown in Fig. 12, the voltage $V_{cp}$ at node ‘cp’ becomes $V_{com} + (V_{off}/2)$ and that $V_{cm}$ at node ‘cm’ becomes $V_{com} − (V_{off}/2)$, where $V_{com} = (V_{cp} + V_{cm})/2$. This is because the feedback loop in the modulator forces both of the input voltages of the comparator, ainpx and ainmx, to be equal.

When offset voltages exist, the voltages $V_{cp}$ and $V_{cm}$ come to differ and a difference arises in the settling time of waveforms between nodes ‘cp’ and ‘cm.’ As a result, the distortion deteriorates. Therefore, it is important to reduce the comparator offset voltage to obtain a good SNDR.

The flicker noise is the other cause of performance deterioration in the SNR of the PSDM due to the small input-signal-voltage at the comparator inputs. The dynamic range at the input of the comparator becomes small when the input-signal-voltage becomes small.

Therefore, both the offset voltage and the flicker noise at the input terminal of the comparator must be taken care of.

4.2 CDS for Low-Voltage Operation

In order to reduce the offset voltage and flicker noise, a MOS transistor with large gate size is used in the input part of the circuit [10]. Moreover, it is better to use PMOS transistors in differential form to further reduce the 1/f noise. On the contrast to this, the comparator needs to operate at high speed, and input transistors should be small in size. An effective method to solve this discrepancy in eliminating the influence of both the offset voltage and 1/f noise is the use of the correlated double sampling (CDS) technique.

CDS is a well known technique, though, we utilized CDS as the solution to alleviate a small signal-voltage problem at the input of the comparator to achieve near-1 V operation. We can-not apply CDS to the conventional PSDM because the voltages of the signal paths are set at $V_{DD}/2$ and the MOS switches become floating switches. The use of differential amplifiers as a part of the comparator also becomes difficult in that case. Of course, it may be possible to use pseudo-differential circuits which do not use the differential pair with the current source for the input differential circuit [4]; however, the gain of the comparator becomes dependent on the voltages at the input terminals.

In contrast to this, as discussed earlier, the voltage of the signal path in our circuit was set to 0.2 V, and MOS switches that are used in CDS circuits turn completely on without becoming floating switches. Moreover, the circuit with a PMOS differential pair and a current source can eas-
Figure 13 shows the comparator circuit with a CDS function. The comparator consists of four stages of a differential amplifier, namely ‘cmpa1,’ ‘cmpa2,’ ‘cmpa3’ and ‘cmpd,’ each with the common-mode feedback circuit. Two more inverters are prepared between the fourth differential amplifier and the latch in order to elevate the voltage gain. The voltage gain $A$ of the differential amplifier is 20 dB, and the offset and the noise, especially the flicker noise, are expected to be reduced by 20 dB and 10 dB, respectively. The comparator does not require feedback, and the dc gain and the $-3$ dB frequency bandwidth become 118 dB and 80 MHz, respectively. The W/L of the input transistor (PMOS) is $20 \mu m/0.18 \mu m$. By using 1/f noise parameters that are obtained from the actual noise measurements of a transistor, the $E_{com}$ value is calculated to be 45uVrms. The capacitors $cp1$ and $cp2$ are both 1 pF. NMOS transistors are used as switches from $sw1$ to $sw6$, and the W/L ratio of each transistor switch is selected to be $32 \mu m/0.18 \mu m$.

5. Experimental Results

5.1 Effect of Eliminating Floating Switches

In order to verify the effectiveness of the proposed PSDM, a PSDM chip using a standard CMOS 0.18-µm process was fabricated and evaluated. The supply voltage was 1.1 V. The output PWM pulses were Fast Fourier Transformed, and the amplitude of each frequency component was displayed. The input signal frequency of the PSDM was 10 kHz, and the clock frequency was 10 MHz. The clock frequency was reduced to 10 MHz so that low-frequency components would properly appear in the FFT results. Figure 14 and Fig. 15 show the two FFT results of two different designs on the same chip. Figure 14 shows the FFT result in a conventional design when the signal path voltage is $V_{DD}/2$. Figure 15 shows the FFT results for our design when the signal path voltage is 0.2 V and floating switches are eliminated. Apparently, the low-frequency noise, distortion, and slope of the noise-shaping curve characteristics shown in Fig. 15 are superior to those in Fig. 14.

Figure 16 shows the SFDR change that occurs with the signal-path-voltage change. When the signal path voltage becomes greater than 0.3 V, the SFDR decreases and unwanted frequency components increase. A signal path voltage of less than 0.3 V is desired for the PSDM to operate from a 1.1 V supply voltage.

5.2 Effect of Utilizing CDS

Figure 17 and Fig. 18 further show the effect of utilizing CDS. These figures were obtained by measuring two different circuits on the same chip. One circuit is the PSDM without CDS whose FFT results are shown in Fig. 17, and the other is the PSDM with CDS whose FFT results are shown in Fig. 18. The unwanted harmonics are seen in Fig. 17 while they are not seen in Fig. 18. This shows the effect of the offset voltage reduction achieved by using CDS.

Figure 19 shows and compares the spectrum of those
shown in Fig. 17 and Fig. 18 in the frequency range from 10 Hz to 100 Hz. The low-frequency noise components are less in our design with CDS compared with the conventional design without CDS.

5.3 Filters and Dynamic Range

A different chip from that of shown in Sects. 5.1 and 5.2 was used because it requires a different evaluation board without the IC socket. Figure 20 shows the designed switched capacitor filter and DAC. Rin, cr1a and cr2a in Fig. 20 are set at 1/3 kΩ, 600 fF and 200 fF, respectively. The minimum capacitor value throughout the circuit is 200 fF, and the total capacitor value in the switched capacitor filter is 95 pF. The DAC switches are CMOS switches, while the other switches are NMOS switches. The size of the NMOS is 32 μm/0.18 μm (W/L), and that of the PMOS is 64 μm/0.18 μm (W/L). The first pole and second pole of this second-order filter are 32 kHz and 136 kHz, respectively, and the zero is 3 MHz, when the sampling frequency fs is 40 MHz.

The chip photograph is shown in Fig. 21. It contains two different designs, one with CDS and the other without CDS. Both designs have no floating switches. The chip size is 2.5 × 2.5 mm² including two designs. The core area of the modulator including clock generator is 0.91 mm² and the total power dissipation is 2.2 mW from a 1.1 V supply voltage.

Figure 22 shows the measured dynamic range when the frequency bandwidths is 40 kHz and the clock frequency is 40 MHz. Table 1 summarizes the overall performance of the test chip.
Although we could observe its operation up to 100 MS/s in a HSPICE simulation, the actual chip is suffered from the impedance of bonding wires at terminals for bias voltage, and relative good performance were obtained up only to 40 MS/s. We prepared an external Vbias terminal for each channel of pseudo-differential configuration as shown in Fig. 23 and Fig. 24. In this case voltages Vbiasp and Vbiasm change when the phase changes form φ1 to φ2. Because the stored charge of C1b in each channel is different and discharge current also become different. This causes unbalance of Vbiasp and Vbiasm. As the comparator input signal is very small, the settling time at Vbiasp and Vbiasm terminals determine the operation speed of the modulator. In order to eliminate the influence of bonding wires, internal Vbiasp and Vbiasm should be connected on the chip or the bias voltage circuit for Vbias should be included on the chip.

Although we attempted 1.0 V operation of the PSDM, the SFDRs deteriorated more than 10 dB in comparison with 1.1 V operation. The on-resistance might have been larger than we expected. As a result, the 1.1 V operation with a 40 MHz clock was chosen for the evaluation. The observed peak SNR was 72 dB, the SFDR was 74 dB, and the dynamic range was 77 dB.

6. Conclusion

The possibility of realizing a near 1 V operational PSDM was examined. By lowering the voltage of the signal paths in a filter, using a linear resistor for the input, modifying the gain both in the feedback data path and the input part, and introducing CDS and offset canceling techniques for a comparator, 1.1 V operation of a PSDM was realized.

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References


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