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LETTER *Special Section on Analog Circuits and Related SoC Integration Technologies*

A Study to Realize a 1-V Operational Passive Σ-Δ Modulator by Using a 90 nm CMOS Process

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SUMMARY A 1-V operational sigma-delta modulator with a second-order passive switched capacitor filter is designed and fabricated by using a 90 nm CMOS process. No gate-voltage bootstrapped scheme is adopted to drive analog switches, and the voltage gain of a comparator is chosen to be 94 dB. The experimental results show that the peak SNR reached 68.9 dB with a frequency bandwidth of 40 kHz when the clock was 40 MHz.

key words: *sigma-delta modulator, 1-V operation, 90 nm CMOS process, second-order passive switched capacitor filter*

1. Introduction

As the supply voltage of LSIs decreases, the supply voltage of analog circuits should also be reduced. In the case of a 90 nm CMOS process, for example, the supply voltage is 1.2 V, and it is expected for future CMOS processes that the supply voltage will become less than 1.0 V [1]. However, the realization of a high-performance analog circuit in such a low supply voltage is extremely difficult. The extensive use of digital logics, therefore, to help an analog circuit achieve better performance under that circumstance has been studied. A passive sigma-delta modulator (PSDM) [2] is one candidate which satisfies the requirements for being the future analog circuit because it is not necessary to use neither OP-amp nor OTA. While the previous study [2] offers 1.5 V operation using 0.13 μm CMOS process, the present paper realizes 1.0 V operation using a 90 nm CMOS process.

2. Block Diagram of a Designed Passive Σ-Δ Modulator

The designed PSDM consist of a second-order passive switched capacitor filter, a comparator, and a latch as shown in Fig. 1. In case of the conventional sigma-delta modulator, the filter is realized by using OP-amps and/or OTAs while the designed PSDM has neither OP-amps nor OTAs in the filter. A second-order low-pass filter in the PSDM is implemented by using switched capacitor techniques, in which only analog switches and capacitors are used. As there is no local feedback loop in the circuit such as that from the output to the input of an OP-amp, high speed operation similar to that of a logic circuit is expected. However, the filter has no positive voltage gain and the signal level at the output at high frequency becomes very small.

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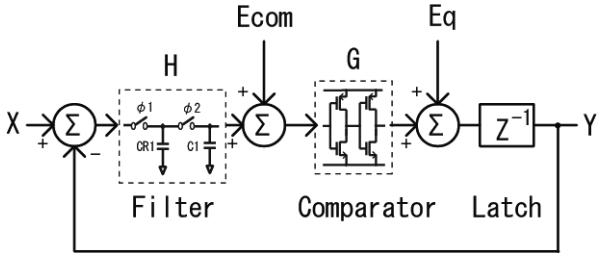

Fig. 1 Block diagram of the designed PSDM.

In order to compensate for the gain loss in the filter part, the voltage gain of a comparator should be high enough to elevate the small signal level at the filter output to the level which is sufficient for quantizing the signal by a latch at half the sampling clock frequency ($fs/2$). At the same time, the equivalent input noise of a comparator (Ecom) should become small relative to the signal level at the filter output.

The overall system transfer function in Fig. 1 becomes

$$Y = X + \frac{Eq}{GH} + \frac{Ecom}{H}, \tag{1}$$

Where Eq is the quantization noise, G is the comparator gain, and H is the transfer function of a filter [3].

3. Circuit Design to Realize 1-V Operation of a PSDM

Although the single-ended version of various circuits is described for the purpose of simplicity, all the designed circuits are configured in a differential manner.

3.1 The Passive Switched Capacitor Filter

Figure 2 shows the second-order passive switched capacitor filter circuit which is used in this PSDM [2]. It is designed to have two poles and one zero in its transfer function. In order to fix the location of the poles and the zero, the equivalent R-C filter is formed. The blocks surrounded by dashed lines in Fig. 2 are replaced by linear resistors such as R1, R2, and R3. MIM (metal insulator metal) capacitors are used in this design. Cr11 and Cr12 have the minimum capacitor value of 200 fF. The input signal is divided in half by using Cr11 and Cr12 before transferring to C1.

The input and output voltage for CMOS swiches are set to 0.5 V and this voltage is the same as the bottom plate voltage of a capacitor, which is indicated by the reverse triangular symbol in Fig. 2. Threshold voltage of MOS transistors are approximately 0.3 V for both NMOS and PMOS,

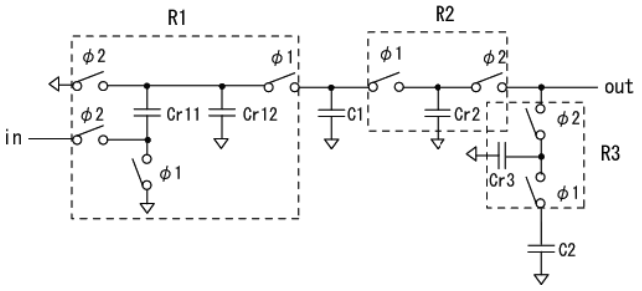

Fig. 2 Equivalent circuit of a passive switched capacitor filter.

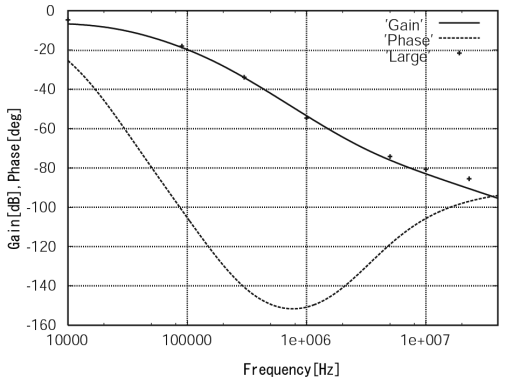

Fig. 3 Frequency response of the equivalent R-C filter and a switched capacitor filter in Fig. 2.

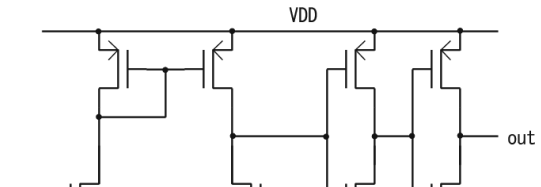

Fig. 4 Equivalent circuit of a comparator.

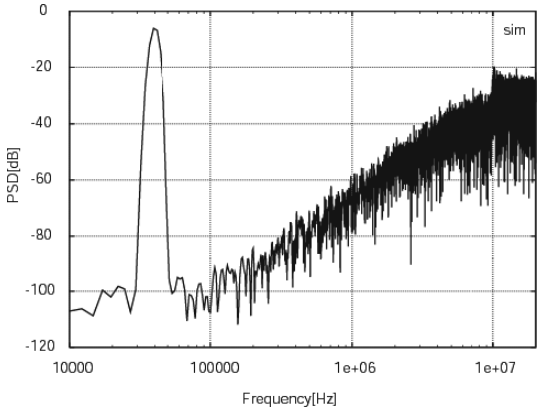

Fig. 5 Simulation result using transistor-level circuits for blocks in Fig. 1.

and care must be taken to maintain the on-resistance of a switch at its minimum. The size of the transitors in a CMOS switch are chosen to be 16 μm/0.1 μm (W/L) for NMOS and 32 μm/0.1 μm for PMOS. Non-overlapping two-phase clock signals are used as $\phi 1$ and $\phi 2$ in Fig. 2.

The simulation results of the voltage gain and phase frequency characteristics of the equivalent R-C filter is shown in Fig. 3. The transient analysis results of the switched capacitor circuit shown in Fig. 2 are also plotted by using crosses in Fig. 3, and its characteristic agrees closely with that of the equivalent R-C filter. Two poles appear at 32 kHz and 134 kHz. Zero appears at 3.1 MHz for ensuring sutability at $fs/2$. Filter gain at $fs/2$ becomes approximately -85 dB. Thus comparator gain needs to be more than 85 dB at $fs/2$.

3.2 Comparator Circuit Design

Figure 4 shows the equivalent circuit of the comparator. A pseudo-differential configuration is adopted for the first stage of an amplifier. This makes 1-V operation of the circuit because it requires Vth plus 2Δ for the minimum supply voltage, where Δ is the minimum drain-to-source voltage of a transistor necessary to maintain operation in saturation region.

The comparator gain needs to be relatively high; however, it is not necessary to be linear throughout the entire frequency range. It is designed to be 94 dB and 240 MHz for the -3 dB frequency. The simulated input-referred noise is 50 μVrms.

3.3 Simulation Result in the Frequency Domain

Figure 5 shows the frequency components obtained from the 16384-point FFT analysis of the simulated Y data in Fig. 1. Real transistor circuits for all the blocks in the Fig. 1 are used in this simulation. The input signal frequency is 40 kHz and the input level is -6 dB of the full-scale, that is, ± 150 mVp-p for each of differential inputs. A SNR of 85 dB for 40 kHz frequency bandwidth is obtained with a 40 MHz clock in this circuit simulation.

4. Experimental Results

The chip performance was examined with a 40 MHz clock. Figure 6 shows the result from the 65536-point FFT analysis of the output data. The output data is captured by using a logic analyzer (HP16500B). Input signal frequency is again 40 kHz and the input signal level is -6 dB (± 150 mVp-p) of the full-scale for each of differential inputs. Measured peak SNR reached 65.4 dB for 40 kHz frequency bandwidth. As the clock frequency is 40 MHz, the over-sampling ratio in this case becomes 500.

The slope for the noise shaping in Fig. 6 is low compared with that in Fig. 5, therefore, the SNR is also low in the case in Fig. 6. This is a problem that needs further investigation.

Figure 7 shows the SNR and SNDR curves vs. the input

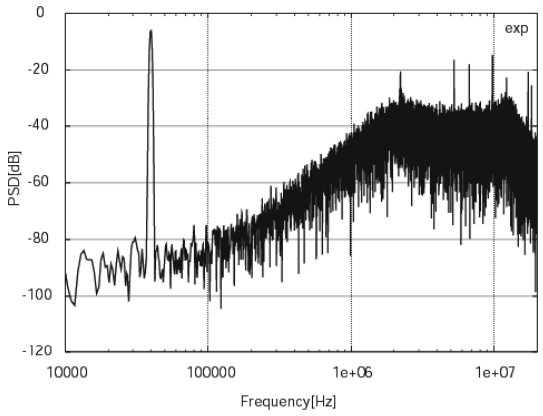

Fig. 6 Experimental result of the system frequency characteristics.

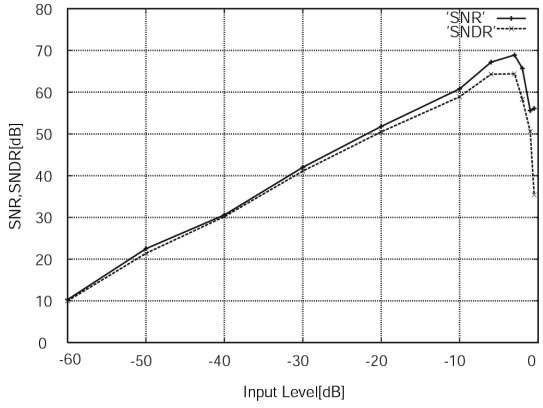

Fig. 7 Measured SNR and SNDR versus input level.

signal level. The input signal frequency is 10 kHz. The measured peak SNR is 68.9 dB and the peak SNDR is 64.4 dB for a 40 kHz frequency bandwidth.

Figure 8 shows a chip micrograph. The chip was fabricated in a standard digital 90 nm CMOS process. The PSDM is configured in differential structure. Switched capacitor and comparator parts are separated from the digital part by guard rings in order to minimize switching noise intruding from the digital parts. The chip core size is $1300\,\mu\text{m} \times 800\,\mu\text{m}$.

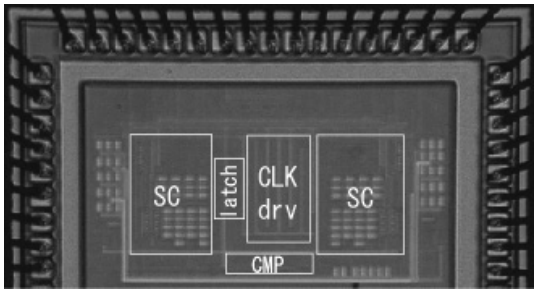

Fig. 8 Chip microphotograph.

5. Conclusion

The characteristics of a 1-V operational passive sigma-delta modulator was examined. 1-V operation has been verified by measuring the peak SNR of 68.9 dB with the frequency bandwidth of 40 kHz and a 40 MHz clock. It has been verified that some of high-performance analog function can be implemented only by logic-based circuits in the sub-$0.1\,\mu$m era without using traditional analog circuits.

Acknowledgments

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