LETTER *Special Section on Analog Circuit and Device Technologies*

A Study to Realize a CMOS Pipelined Current-Mode A-to-D Converter for Video Applications

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SUMMARY The possibility of realizing a CMOS pipelined current-mode A-D converter (ADC) for video applications has been examined. Two times the input current is obtained at the output of a bit-block of a pipelined ADC by subtracting the negative output current from the positive output current in the pseudo-differential configuration. Subtraction of the sub-DAC (D-to-A converter) current from the two times the input current is performed by controlling of the current comparator, which compares the positive and the negative input currents. A prototype chip has been implemented using 0.35 μm CMOS devices. It operates in 28 MS/s, and showed a 42 dB signal-to-noise ratio from the 2 V supply voltage.

key words: *current-mode circuit, pipelined ADC, low-voltage, high-resolution*

1. Introduction

Device sizes have continued to be reduced. Although the performance requirements for analog circuits are stringent, they are required to operate with a reduced voltage supply. It is time for us to reconsider a circuit design methodology to fit reduced-size of the devices.

The current-mode circuit approach has been considered to be a candidate for the new analog circuit design methodology in the sub-0.1 μm era, because the impedance of each node becomes low; therefore, a low-voltage, high-speed operation is expected [1]. However, the precision of the transferred and processed current is poor because of the terminal voltage difference, the V_{th} variation and β variation of the transistors. To date, 6-bit and 8-bit implementations have been achieved for high-speed ADCs using the current-based approach [2]–[4]. However, the 8-bit implementation used the calibration method to maintain accuracy [4].

The above facts can be viewed as having shown that current-mode circuits have poor accuracy. We believe that the current-mode circuit approach could achieve high accuracy and become more effective in low-voltage applications, which match well with the voltage constraints imposed on future analog circuits. For this reason, we have examined the possibility of realizing the current-mode ADC for video applications with less than 2 V of supply voltage. We have designed, fabricated and tested a prototype ADC chip by using 0.35 μm CMOS devices, and the results of this test are reported below.

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2. The Bit-Block Circuit of a Current-Mode Pipelined ADC

The ADC performs a pipelined operation and has a 1.5-bit bit-block architecture. However, this architecture was initially developed for voltage-mode circuits [5]. In this paper, we propose the current-mode circuit shown in Fig. 1, which is a bit-block circuit that performs a pipelined operation and realizes a 1.5-bit bit-block operation. The sample and hold operation of the input current is done by the sample switches SWSH1 and SWSH2 and the sample capacitors CH1 and CH2. The gate voltage of the transistors at the time when the switches are turned off is stored in the sample capacitors CH1 and CH2, and the hold operation becomes possible. However, this type of circuit operation often suffers from clock-feedthrough from sample switches, and this introduces serious current error. The circuit is configured in pseudo-differential form so that the clock-feedthrough produced in channel 1 is cancelled by that in channel 2, and vice versa.

In addition to this, the current relationship between the output and the input, that is, $2I_{in} \mp I_{REF}$, should be implemented. Here, I_{REF} equals half of the full-scale current value: that is, 200 μA in case of Fig. 1. When $+I_{in}$ and $-I_{in}$ are applied to the pin and nin terminals in Fig. 1, $+I_{in}$ flows in Mp1, Mp2 and Mp5, while $-I_{in}$ flows in Mp3 and Mp4 in channel 1, and $-I_{in}$ flows in Mn1, Mn2 and Mn5, while $+I_{in}$ flows in Mn3 and Mn4 in channel 2. Transistors $M_{p1} \sim M_{p5}$ and $M_{n1} \sim M_{n5}$ are identical. Those resistors that are transistors in the triode region in reality, $r_{p1} \sim r_{p5}$ and $r_{n1} \sim r_{n5}$, are also identical. As a result, two times the current flow relative to the input signal current is obtained such that $2I_{in}$ flows out from the $CH1_{out}$ terminal, and $2I_{in}$ flows into the $CH2_{out}$ terminal. By comparing the currents of both channels, current comparators activate sub-DAC currents ($I_{DAp1}, I_{DAp2}, I_{DAn1}$ and I_{DAn2}). A sub-DAC current is set to 200 μA, which is equal to I_{REF}. As a result, $2I_{in} \mp I_{REF}$ is obtained at the pout terminal. In the same manner, $-2I_{in} \pm I_{REF}$ appears at the nout terminal.

In order to maintain the accuracy of the transferred currents, each node voltage is kept constant by the voltage-mode operational amplifiers A1 and A2. As pout and nout connect to the inputs of the next bit-block, their node volt-

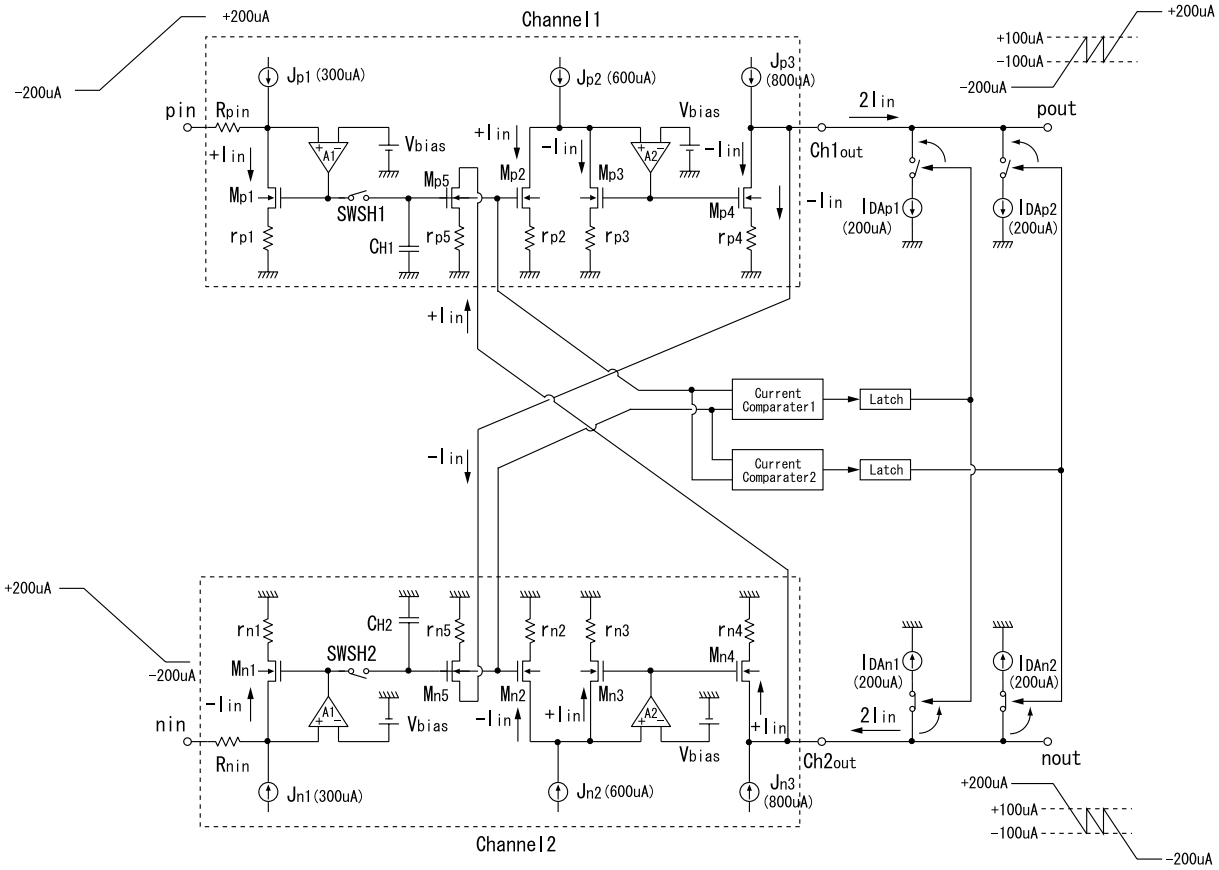

Fig. 1 The 1.5-bit bit-block circuit.

ages are also fixed. The voltage gain of A1 and A2 need not be too high, because their outputs are connected to gates of current-mirror transistors, whose voltage changes are already suppressed to some extent. However, the conventional differential-type amplifier is used for these voltage-mode operational amplifiers in this design, and this limits the minimum supply voltage to 2 V. The degeneration resistors ($r_{p1} \sim r_{p5}$, and $r_{n1} \sim r_{n5}$) improve the current transfer ratio between the transistors due to threshold mismatches [6]. In the first bit-block, the positive and negative input signal voltages are voltage-to-current converted by input resistors. This is a simple and precise conversion method. In this way, the bit-block of a current-mode pipelined ADC is configured.

3. Evaluation Results of the Prototype ADC

The current-mode ADC was designed and fabricated using 0.35 μm CMOS devices. Figure 4 is a chip microphotograph. The chip is originally intended to realize a 12-bit resolution; however, some of the DC bias voltages did not coincide with those of circuit simulation. Nevertheless, A-D converted data were available and could be evaluated to some extent. The 10-bit DAC was used to evaluate the ADC's digital output data by converting it into an analog waveform.

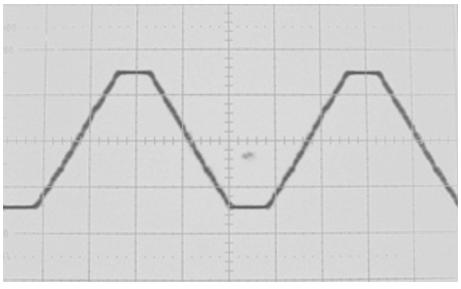

Fig. 2 The reconstructed output waveform.

Figure 2 shows the output waveform. The full scale input voltage is ±400 mV, and the input resistor value is 2 kΩ. The supply voltage is 2 V, and the clock frequency is 28 MHz. A large input signal of 10 kHz was applied, and the output waveform become clipped. About 7-bit equivalent linearity has been obtained.

Figure 3 shows the frequency spectrum when a 1 MHz, −10 dB of full-scale input signal was applied. The clock frequency was 28 MHz, and the supply voltage was 2 V. It is necessary to improve the distortion in the future. The SFDR was only 37 dB. However, the signal-to-noise ratio become 32 dB for a 14 MHz frequency bandwidth with −10 dB of full-scale input signal. This means that the S/N reached 42 dB in full-scale-level equivalent terms, and was 7-bit

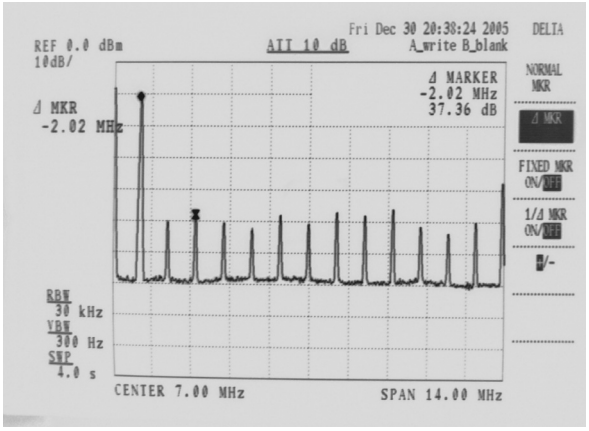

Fig. 3 The frequency spectrum of a 1 MHz reconstructed output waveform.

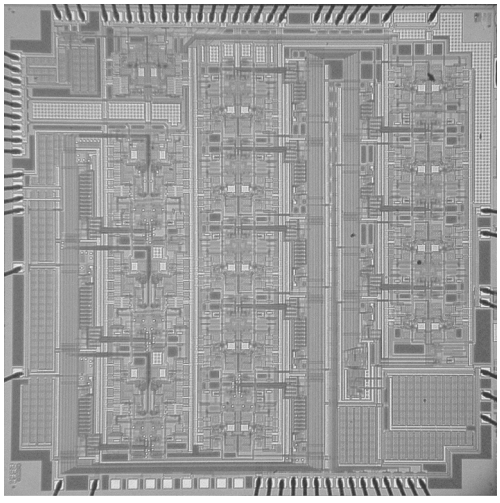

Fig. 4 The chip microphotograph.

equivalent.

Although the current-mode circuit is expected to operate at high frequency, the maximum clock frequency was limited to 28 MHz in this case. One reason was that several feedback loops using operational amplifiers were introduced in this design to obtain good matching of the current. When the phase margin of the loop is small, damping occurs at nodes whose voltage is fixed by operational amplifiers when the sample-and-held signal changes. It takes time for these nodes to settle down.

4. Conclusion

The above evaluation results show that a 7-bit equivalent current-mode ADC has been realized although several improvements in areas such as clock speed, distortion, and linearity remain to be made. We would like to realize a more than 10-bit equivalent current-mode ADC in the near future.

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