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PAPER Special Section on Analog Circuit Techniques and Related Topics

Analysis and Design of a Current-Mode PWM Buck Converter Adopting the Output-Voltage Independent Second-Order Slope Compensation Scheme

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SUMMARY In this paper, we propose the use of second-order slope compensation for a current-mode PWM buck converter. First, the current feedback loop in a current-mode PWM buck converter using a conventional slope compensation is analyzed by the small-signal transfer function. It becomes clear that the stability and frequency bandwidth of the current feedback loop is affected by the external input voltage and the output voltage of the converter. Next, the loop with second-order slope compensation is analyzed, and the result shows that the loop becomes unconditionally stable with the adoption of second-order slope compensation with appropriate parameter values and a current sensing circuit whose current is sensed across an impedance that is inversely proportional to the input voltage. In order to verify our theory, we designed whole circuits of a current-mode PWM buck converter including the new inductor current sensing circuit and the second-order voltage generator circuit using device parameters from the 0.6 μm CMOS process. The circuit simulation results under the conditions of 4 MHz switching frequency, 3.6 V input voltage and 2.4 V output voltage are presented.

key words: *PWM buck converter, current-mode control, slope compensation*

1. Introduction

Today, various mobile equipment has become available due to the explosion of the applications in the wireless communication field. The use of step-down DC-DC converters is necessary in this equipment to convert the battery voltage to the LSI's supply voltage. Of course, power efficient converters are needed in order to extend battery lifetimes.

There are two control methods for the PWM DC-DC converter, the voltage-mode and current-mode. The voltage-mode control has the disadvantage of a small frequency bandwidth. The external inductor and capacitor at the output, which form a low-pass filter, introduce 180° phase shift at the self-resonant frequency; that is, $f_{LC} = 1/2\pi\sqrt{LC}$. This requires a gain of the control loop to be less than unity at f_{LC} to guarantee stability. The result is a slow response in output voltage or current change [1].

On the other hand, the current-mode control can realize a large frequency bandwidth. Two loops are needed in this configuration: the conventional voltage control loop and the current control loop. Though circuits become complicated, it is possible to extend the frequency bandwidth up to half of the switching frequency [2]–[5]. In order to guarantee the stability of the system, the slope compensation is usually introduced. The amount of slope compensation is important because it affects both on stability and the frequency bandwidth. But the optimum value of slope compensation varies depending on external input voltage and the output voltage of the DC-DC converter.

This paper proposes the use of second order slope compensation to make the slope value independent of the external input voltage and the output voltage of the converter. In Sect. 2, a block diagram of the designed current-mode PWM buck DC-DC converter is shown. Section 3 analyzes the current feedback loop of the conventional converter by adopting the small-signal transfer function, and describes the relationship between the slope value and the stability. Section 4 analyzes the effectiveness of the second order slope compensation in terms of the stability and frequency bandwidth. The newly designed circuits to form the proposed PWM buck DC-DC converter appear in Sect. 5. Section 6 compares the hand calculation result and the SPICE simulation result of the circuits. Section 7 concludes this study.

2. Block Diagram of the Designed Current-Mode PWM Buck DC-DC Converter

Figure 1 shows a block diagram of the designed PWM buck DC-DC converter with current-mode control. It consists of an error amplifier, a PWM comparator, an SR-FF, a reference voltage generator, a current sensing circuit, a control circuit, a slope compensation circuit, and power MOS transistors M_p and M_n. The inductor L, capacitor C, load resistor R_L and feedback resistors R_{f1} and R_{f2} are all external. The converter has two control loops, a voltage control loop and a current control loop. The current sensing circuit detects the inductor current, then converts it into voltage. This voltage, after including the slope compensation voltage, is applied to a comparator and is compared with the one from the error amplifier in the voltage control loop.

At the beginning of the clock period, a set pulse is applied to the S terminal of SR-FF and this forces Q output high. The output of the control circuit then becomes low,

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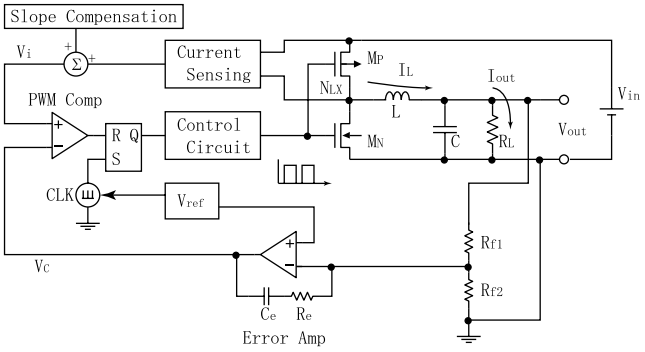

Fig. 1 Block diagram of a PWM buck DC-DC converter with the current-mode control.

and M_p turns on and M_n turns off. As a result, the inductor current I_L begins to increase with time. When V_i in Fig. 1, which becomes proportional to the inductor current, exceeds V_c, the comparator output becomes high and therefore resets the Q output of SR-FF low. Then, M_p turns off and M_n turns on. Let's assume the output current I_{out}, which flows through load resistor R_L, suddenly becomes small due to undesirable disturbance. Then, the inductor current I_L decreases and V_i decreases. As the rate of increase I_L with M_P on is constant, assuming that the input voltage V_{in} and the output voltage V_{out} don't change, the required time for V_i to exceed V_c increases. This makes M_p's turn-on time long. The longer the turn-on time of M_p becomes, the larger I_{out} becomes. In this way, the output current is kept constant. Moreover, when I_{out} decreases, V_{out} slightly drops and the output of the error amplifier, in other words V_c, increases. The required time for V_i to exceed V_c is expected to become much longer.

3. Small-Signal Transfer Function and the Stability of the Conventional Current Feedback Loop

To analyze the current feedback loop of the PWM converter, a small signal transfer function of the current feedback loop is established. Figure 2 shows waveforms of V_c and V_i when the conventional slope compensation signal is applied. Figure 3 shows the block diagram of the current feedback loop. In Fig. 2, Z_{cf} stands for the current-to-voltage conversion trans-impedance gain of the current sensing circuit; m_c is the voltage slope of the slope compensation signal; T_s is one clock period; D is the duty which is the ratio between the interval of M_p being on and T_s; and Δd is the change in duty. m_1 is the slope of the inductor current change and it becomes

$$m_1 = \frac{V_{in} - V_{out}}{L} \tag{1}$$

Suppose that V_c changes by Δv_c as shown in Fig. 2. Then, the on-time duration of V_i changes by $\Delta d \times T_s$ and is calculated as,

$$\Delta d T_s = \frac{\Delta v_c}{m_1 Z_{cf} + m_c} \tag{2}$$

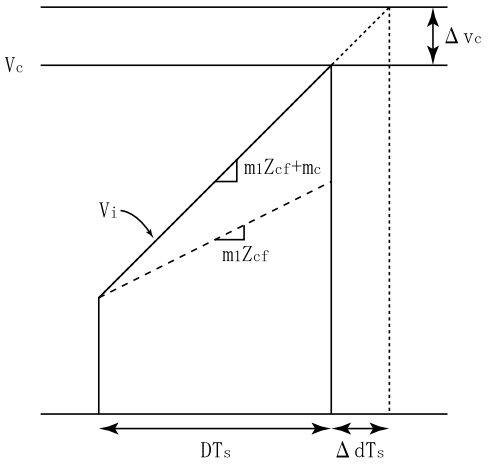

Fig. 2 Waveforms of V_c and V_i in a current control loop.

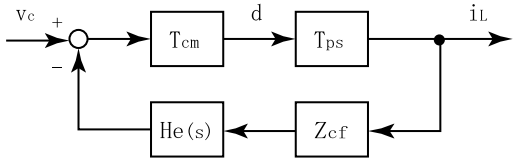

Fig. 3 Block diagram of a current feedback control loop.

This gives the small-signal transfer function T_{cm} between the control signal V_c and the duty D as shown in Fig. 3:

$$T_{cm} = \frac{\Delta d}{\Delta v_c} = \frac{f_s}{m_1 Z_{cf} + m_c} \tag{3}$$

where $f_s = 1/T_s$. In Fig. 3, T_{ps} shows the small-signal transfer function between the duty and the inductor current, described as a PWM power-stage model in reference 1 and reference 6. Using that model, T_{ps} becomes

$$T_{ps} = \frac{\Delta i_L}{\Delta d} = \frac{V_{in}}{Z_{LCR}} \tag{4}$$

$H_e(s)$ is the sampled-data transfer function which is appeared in reference 3. In the PWM converter with voltage-mode control, the frequency bandwidth of the control loop becomes far smaller than the switching frequency; therefore, $H_e(s)$ is approximated to 1. On the other hand, the frequency bandwidth of the current-mode control loop is large, and $H_e(s)$ should be considered as it is. According to reference 3,

$$H_e(s) = \frac{sT_s}{e^{sT_s} - 1} \tag{5}$$

For the purpose of simplicity, the second-order approximation is usually used.

$$H_e(s) \cong 1 + \frac{s}{w_n Q_z} + \frac{s^2}{\omega_m^2} \tag{6}$$

where $\omega_n = \pi f_s$ and $Q_z = -2/\pi$ in reference 3, or $\omega_n = \sqrt{12} f_s$ and $Q_z = -1/\sqrt{3}$ in reference 4. This approximation is valid up to half of the switching frequency. Eq. (6) has a

second-order pole at $f = f_s/2$ when we adopt ω_n and Q_z in reference 3.

It is well known that the current feedback loop without slope compensation becomes unstable when the duty becomes larger than 50%. Therefore, the slope compensation must be included. However, the stability and the frequency bandwidth of the current feedback loop largely depend on the value of slope compensation.

The closed-loop transfer function of the current feedback loop in Fig. 3 becomes

$$T_{cl} = \frac{\Delta i_L}{\Delta v_c} = \frac{T_{cm} \cdot T_{ps}}{1 + Z_{cf} \cdot H_e(s) \cdot T_{cm} \cdot T_{ps}} \tag{7}$$

Here, we assume for simplicity that the voltage across the inductor is kept constant; therefore, the approximation $Z_{LCR} \cong sL$ holds. Then, substituting equations (3), (4) and (6) into equation (7) yields

$$T_{cl} = \frac{1}{Z_{cf}} \cdot \frac{1}{1 + \frac{2s}{\omega_n}\zeta + \frac{s^2}{\omega_n^2}} \tag{8}$$

where the damping factor ζ is

$$\begin{aligned} \zeta &= \frac{\pi L}{2V_{in}Z_{cf}}\left(m_1 Z_{cf} + m_c\right) - \frac{\pi}{4} \\ &= \frac{\pi}{2}\left(\frac{1}{2} + \frac{L}{V_{in}Z_{cf}}m_c - \frac{V_{out}}{V_{in}}\right) \end{aligned} \tag{9}$$

In general, V_{out}/V_{in} is interpreted as duty D.

The stability is deeply related to the ζ value in equation (9). The current feedback loop becomes unstable when ζ becomes negative due to the fact that pole positions of equation (8) fall in the right half plane. Therefore, the necessary condition to stabilize this feedback loop is that ζ must be positive. Figure 4 shows the frequency characteristics of equation (8). When ζ becomes close to zero, a significant peak arises in gain characteristic at half of the switching frequency, where the switching frequency f_s is 4 MHz. This is because of the second-order pole appearing in equation (8). This undesirable instability is called a sub-harmonic oscillation. In order to suppress this peak, it is necessary to make the value of the second term in the denominator of equation (8) less than unity at the frequency that is half of the switching frequency. This yields $\zeta > 1/2$. Moreover, when ζ becomes larger than one-half, the frequency bandwidth of the current feedback loop decreases. When $\zeta = 5$, the -3 dB frequency becomes approximately one-tenth as seen in Fig. 4.

From equation (9), the m_c that satisfies the relation $\zeta > 1/2$ is calculated as:

$$m_c > \frac{Z_{cf}}{L}\left\{\left(\frac{1}{\pi} - \frac{1}{2}\right)V_{in} + V_{out}\right\} \tag{10}$$

The required m_c depends both on V_{in} and V_{out}. The influence of V_{out} is about five times larger than that of V_{in}. We need to set m_c at the maximum in order to satisfy equation (10) all the time whenever V_{out} changes. The worst-case condition

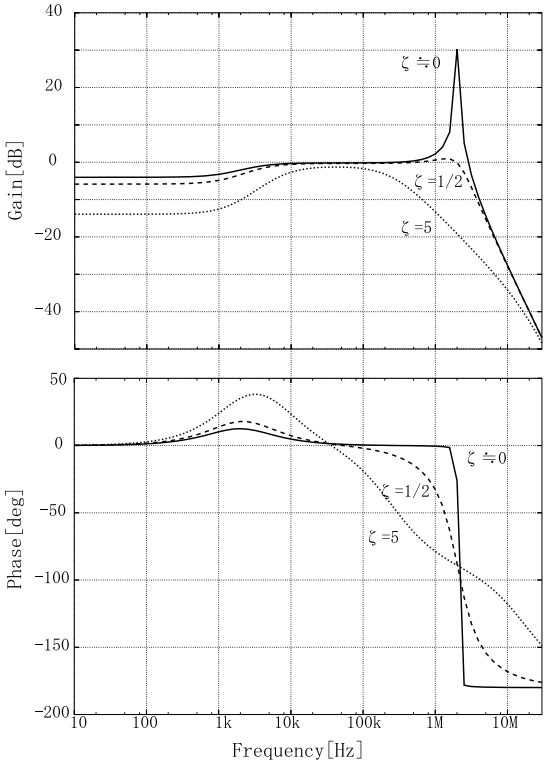

Fig. 4 Closed-loop transfer function of the current feedback loop.

is given when $D = 1$ and V_{out} are the specified maximum value, that is, $V_{out} = V_{outm}$.

$$m_c = \frac{Z_{cf}V_{outm}}{L}\left\{\left(\frac{1}{\pi} + \frac{1}{2}\right)\right\} \tag{11}$$

Substituting equation (11) into equation (9) gives a ζ value. Note that V_{outm} is the fixed maximum value that is decided by considering the possible output voltage range of the converter. V_{out} of less than V_{outm} is usually taken. Assume that $V_{out} = \frac{1}{5}V_{outm}$. The calculation indicates that ζ changes from 3.2 to 5.6 according as duty D changes from 0.5 to 1. The change of the ζ value caused by duty D change results in the change in the frequency bandwidth as can be seen in Fig. 4. Moreover, it might happen that the ζ value becomes more than 5.

4. Stability with the Second-Order Slope Compensation

In order to avoid the stability dependence on the output voltage V_{out}, we propose using a second-order slope compensation scheme.

Figure 5 shows the V_c and V_i for the PWM comparator when the second-order slope compensation is used. In steady state,

$$V_c = m_1 Z_{cf} D T_s + m'_c (D T_s)^2 + V_{base} \tag{12}$$

where m'_c is the coefficient of the second-order slope compensation voltage, and V_{base} is the voltage of V_i at time zero.

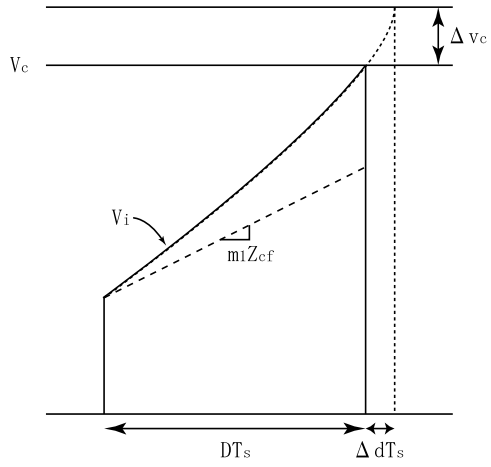

Fig. 5 Waveforms of V_c and V_i in a current control loop (second-order slope compensation).

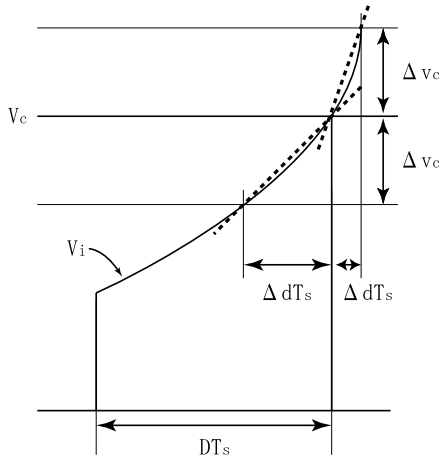

Fig. 6 The slope necessary to perform the effective slope compensation for a large disturbance.

When V_c increases by Δv_c, we obtain

$$V_c + \Delta v_c = m_1 Z_{cf}(D + \Delta d) T_s + m'_c (D + \Delta d)^2 {T_s}^2 + V_{base} \quad (13)$$

Assuming that Δd is sufficiency small compared with D, equation (13) becomes

$$V_c + \Delta v_c \cong m_1 Z_{cf}(D + \Delta d) T_s + m'_c (DT_s)^2 \left(1 + \frac{\Delta 2d}{D}\right) + V_{base} \quad (14)$$

The small-signal transfer function T_{cm2} between D and V_c when the second-order slope compensation is used becomes

$$T_{cm2} = \frac{\Delta d}{\Delta v_c} = \frac{f_s}{m_1 Z_{cf} + 2DT_s m'_c} \quad (15)$$

Substituting equation (15) into equation (7), the small-signal transfer function of the whole current feedback loop T_{cl2} becomes

$$T_{cl2} = \frac{1}{Z_{cf}} \cdot \frac{1}{1 + \frac{2s}{\omega_n}\zeta + \frac{s^2}{\omega_n^2}} \quad (16)$$

where the damping fuctor ζ changes to

$$\zeta = \frac{\pi L}{2V_{in}Z_{cf}} \left(m_1 Z_{cf} + 2DT_s m'_c\right) - \frac{\pi}{4} \quad (17)$$

As previously mentioned, ζ must be more than one half in order to avoid a peak in loop gain at half the switching frequency. This yields m'_c as

$$m'_c > \frac{V_{in}Z_{cf}f_s}{2L}\left\{1 + \left(\frac{1}{\pi} - \frac{1}{2}\right)\frac{1}{D}\right\} \quad (18)$$

Equation (18), however, is the one that is only valid when the control loop is close under the steady-state condition. In order to guarantee stability, it is necessary to consider the case when a large amount of disturbance is introduced; the voltage slope of V_i for a large disturbance is different from that of a small disturbance because the slope is a second-order function.

Figure 6 shows the slope values needed to perform the effective compensation when a large amount of disturbance is introduced. They are shown in the figure with dashed lines connected between the start-point and the end-point of disturbance. We denote the effective slope value of the slope compensation as $m_{c(eff)}$. When V_c increases (or I_L decreases), $m_{c(eff)}$ becomes larger than $2DT_s m'_c$, which is the value close under the steady state condition. On the other hand, when V_c decreases (or I_L increases), $m_{c(eff)}$ becomes smaller. The minimum value of $m_{c(eff)}$, which occurs when DT_S equal ΔdT_s, is given by

$$m_{c(eff)min} = \frac{m'_c (DT_s)^2}{DT_S} = m'_c (DT_s) \quad (19)$$

This means that we need to redefine ζ in equation (17) to be

$$\zeta = \frac{\pi L}{2V_{in}Z_{cf}} \left(m_1 Z_{cf} + DT_s m'_c\right) - \frac{\pi}{4} \quad (20)$$

in order to find the effective m'_c under this large disturbance condition. Note that ζ in equation (17) always becomes larger than that of equation (20).

Even when a large disturbance occurs, the system should be stable, though the occurrence is rare. We would like to guarantee this stability by assigning m'_c a value which makes the ζ value in equation (20) positive. This leads to

$$m'_c > \frac{V_{in}Z_{cf}f_s}{L}\left(1 - \frac{1}{2D}\right) \quad (21)$$

Therefore, we choose the m'_c value by using $D = 1$ to be

$$m'_c = \frac{V_{in}Z_{cf}f_s}{2L} \quad (22)$$

Equation (22) does not contain the output voltage. Substituting equation (22) into equation (17) gives a ζ value close under that of the steady-state condition.

$$\zeta = \frac{\pi L}{2V_{in}Z_{cf}}\left(\frac{V_{in}-V_{out}}{L}Z_{cf}+\frac{V_{in}Z_{cf}D}{L}\right)-\frac{\pi}{4}$$
$$= \frac{\pi}{2}-\frac{\pi}{4}=\frac{\pi}{4}\cong 0.8 \quad (23)$$

The result indicates that the ζ value, in other words, the frequency bandwidth of the loop under a small disturbance condition close to the steady state, does not change all the time. We come to set the m'_c value which realizes the constant ζ value for a small disturbance, yet guarantees stability in a large-disturbance condition.

5. A Method for Sensing Inductor Current and Slope Compensation

Using the second-order compensation enables the m'_c value to be independent of the output voltage, and realizes a constant frequency bandwidth for the control loop. As can be seen in equation (22), however, m'_c still depends on the input voltage V_{in}. The ultimate goal for m'_c is for it to depend on neither V_{in} nor V_{out}. The independence from V_{in} is realized by configuring the circuit as described below.

Figure 7 shows a circuit that senses the inductor current and produces the second-order slope compensation signal. In order to detect the inductor current, the voltage difference between a drain and a source terminal of power PMOS transistor (M_p) is used. The advantage of this sensing method is that it does not require a resistor in series with the PMOS transistor. The power consumption, therefore, is minimized. When M_p turns on, it is in a linear region and the equivalent resistor value across the drain and the source terminals becomes

$$R_{onP} = \frac{1}{\beta_P (V_{in}-V_{thP})} \quad (24)$$

where β_P and V_{thP} are the transconductance parameter and the threshold voltage of M_p, respectively.

Substituting equation (24) for Z_{cf} in equation (22), we obtain

$$m'_c = \frac{f_s}{2L\beta_P}\cdot\frac{V_{in}}{V_{in}-V_{thP}} \quad (25)$$

If $V_{in} > V_{thP}$, then the V_{in} dependence in equation (25) is eliminated.

When M_P turns on, SW_1 turns on and SW_2 turns off, as shown in Fig. 7. The inductor current I_L, which flows through M_P, produces the voltage at terminal N_{LX}, and this voltage is applied to the source of M_{c1}. M_{c1} is biased by the constant current I_{b1}. So the voltage at N_{LX} is mirrored to the voltage across the resistor R_{c1}. The voltage across the resistor R_{c2} then becomes R_{c2}/R_{c1} times the voltage at N_{LX} in inverted form when the transconductance of M_{c2} is larger than $1/R_{c1}$. Consequently, the conversion gain of the current detection circuit Z_{cf} is

$$Z_{cf} = \frac{R_{c2}}{R_{c1}}\cdot\frac{1}{\beta_P (V_{in}-V_{thP})} \quad (26)$$

When M_P is cut off, SW_1 turns off and SW_2 turns on. The source terminal of M_{c1} is connected to the power line, and only a small amount of constant current flows through M_{c2} in this case. The frequency bandwidth of this circuit is sufficiently higher than the switching frequency in order to sense the complete waveforms of the inductor current. The gain is several-fold. The average current that flows through this circuit is less than ten micro-amperes.

The Slope compensation circuit consists of M_{c3}, M_{c4}, a constant bias current I_{b2}, a capacitance C_c, and a switch SW_3. I_{b2} is stabile, and the slope produced by I_{b2} and C_c is relatively precise. When M_P turns on, SW_3 turns off. The constant current flows through C_c and M_{c3}, and a voltage drop of C_c increases linearly with time. This linear voltage change is applied to the gate terminal of M_{c4}. As a result, a current with a square relationship with time flows in M_{c4} and is converted to square voltage by the resistor R_{c2}. The coefficient of the second-order slope compensation m'_c approximately becomes

$$m'_c = \frac{R_{c2}\beta_{c4}}{2}\times\left(\frac{I_{b2}}{C_c}\right)^2 \quad (27)$$

where β_{c4} is the transconductance parameter of M_{c4}. All the parameters in equation (27) must be selected to satisfy

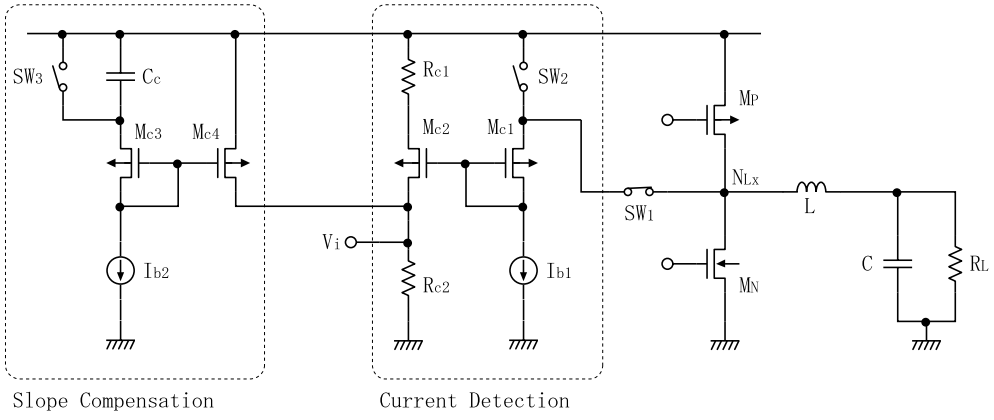

Fig. 7 Current sensing and second-order slope compensation circuit.

equation (25) provided that V_{in} is greater than V_{thP}.

The switch timing of the circuit in Fig. 7 is important. When M_P turns on, a large amount of initial current flows through M_P and a voltage spike appears at terminal N_{LX}. This is considered to be introduced by the parasitic inductor that exists at the source terminal of M_P and by the feed-through current flowing through the parasitic capacitors of M_P and M_N. The spike noise inadvertently resets RS-FF and leads to miss-operation.

In order to avoid the influence of the spike noise, switch timings for SW_1 and SW_2 has been modified. When M_P is cut off, SW_1 is set cut off and SW_2 is set on. Just after M_P turns on, SW_2 is kept on while SW_1 becomes turned on. At this moment, the source terminal of M_{c1} connects to the power line, so that no spike noise at terminal N_{LX} is transferred to the resistor R_{c2}. After a certain period of time, when the spike noise ceases, SW_2 begins to turn off.

6. Estimation of the Overall Frequency Characteristics of the PWM Buck DC-DC Converter with Current-Mode Control

The PWM buck DC-DC converter with current-mode control is designed and its control-loop transfer function is analyzed using following parameters from the actual design.

$$f_s = 4\,\text{MHz} \quad L = 2.2\,\mu\text{H} \quad C = 10\,\mu\text{F} \quad R_L = 20\,\Omega$$
$$\beta_P = 0.7\,\text{S/V} \quad V_{thP} = 0.8\,\text{V} \quad R_{c1} = 10\,\text{k}\Omega \quad R_{c2} = 30\,\text{k}\Omega$$
$$I_{b2} = 3\,\mu\text{A} \quad C_c = 4\,\text{pF} \quad \beta_{c4} = 0.7m\,\text{S/V}$$

Figure 8 shows the small-signal equivalent circuit of a whole PWM buck DC-DC converter with current-mode control. For simplicity, we assume that the input voltage and the reference voltage don't change in time. This means that the voltage feedfoward terms that are described in reference 5 are neglected. $Z_{CR}(s)$ is the combined impedance of C and the load resistor R_L. As the output of the converter is in the voltage form, $Z_{CR}(s)$ is needed to convert the inductor current to the output voltage. It is given by

$$Z_{CR}(s) = \frac{R_L(1 + j\omega R_c C)}{1 + j\omega(R_L + R_c)C} \tag{28}$$

where $R_c(0.3\,\Omega)$ is the series resistance of C.

For the first step, we calculated the transfer function between v_c to v_{out} to see whether sub-harmonic oscillation occurs and whether the frequency bandwidth becomes constant even with changes in the input voltage V_{in} applied to the converter and the output voltage V_{out} derived from the converter. Fig. 9 shows the frequency characteristics of the voltage gain and the phase with different values of V_{in} and V_{out}. The transfer function between v_c to v_{out} becomes the product of equation (16) and equation (28). Equation (28) is similar to the transfer function of the lag-lead filter. No sub-harmonic oscillation is seen in Fig. 9. Although the voltage gain changes slightly depending on V_{in}, the phase of the loop does not change at all. This means that curves of the voltage gain in Fig. 9 all have the same frequency bandwidth of $f_s/2$, where f_s is 4 MHz. The voltage gain dependency derives from the Z_{cf} change as seen in equation (26).

Next, the transfer function of the whole control loop shown in Fig. 8 is calculated. Figure 10 shows the frequency characteristics of the loop from v_{out} to v_{out}, which is the open-loop transfer function. In this case, the voltage feedback loop, which is composed of β and $A_{err}(s)$ in Fig. 8, is added to the analysis that is performed in Fig. 9. The circuit of this voltage feedback loop is already shown in Fig. 1. $\beta(0.21)$ is the voltage-dividing ratio by resistors $R_{f1}(380\,\text{k}\Omega)$ and $R_{f2}(100\,\text{k}\Omega)$. $A_{err}(s)$ is the small signal transfer function of the error amplifier; it is determined by a capacitor $C_e(20\,\text{pF})$ and a resistor $R_e(1200\,\text{k}\Omega)$ in series between the output terminal and the negative input terminal of the error amplifier. V_{in} and V_{out} are chosen to be 3.6 V and 2.4 V, respectively.

Figure 10 also ensures the stability of the loop in that no sub-harmonic oscillation is seen. As the bandwidth of

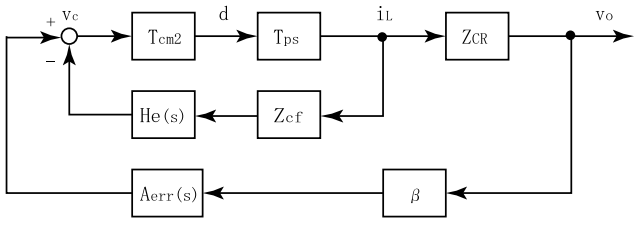

Fig. 8 Small-signal equivalent circuit of the whole PWM buck DC-DC converter with current-mode control.

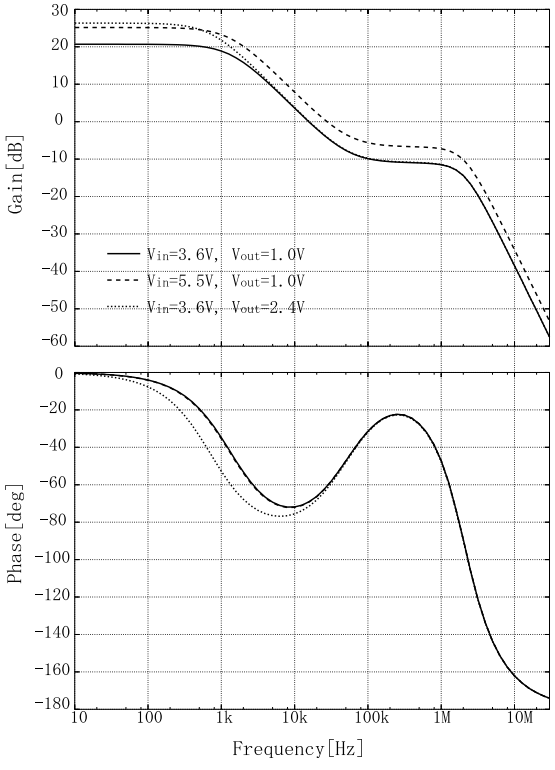

Fig. 9 Frequency characteristics of the current feedback loop of the designed PWM buck DC-DC converter.

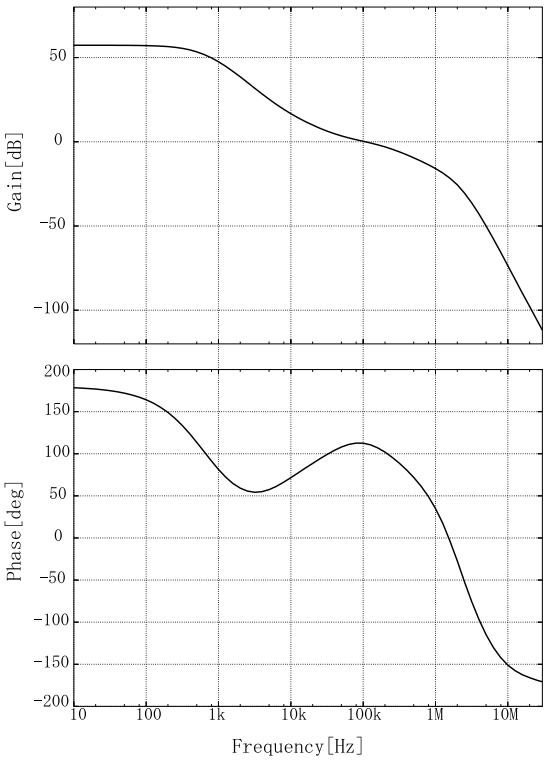

Fig. 10 Open loop transfer function characteristics of the designed PWM buck DC-DC converter with current-mode control.

the voltage feedback loop is chosen to be small relative to $f_s/2$ so that it does not cause the degradation of the loop's stability, the voltage gain from v_{out} to v_{out} also decreases at a frequency below $f_s/2$. However, note that this degradation is due to the voltage feedback loop and that no degradation occurs in the current feedback loop. The gain margin at the frequency where the phase shift becomes 180 degrees is about 20 dB as shown in Fig. 10.

7. Simulation Results

A SPICE simulation has been carried out in order to establish the correct and stable operation of the designed PWM buck DC-DC converter using 0.6 μm CMOS device parameters. Figure 11 shows the results. V_{in} and V_{out} are chosen to be 3.6 V and 2.4 V, respectively. Figure 11(a) shows voltage waveforms at terminal N_{LX} with a solid line and at V_{out} with a dashed line shown in Fig. 1. Fig. 11(b) shows the waveform of the current that flows through the external inductor L. No undesired phenomena such as sub-harmonic oscillation can be seen. Fig. 11(c) shows voltage waveforms of V_i with a solid line and V_c with a dashed line shown in Fig. 1; V_i is the combined voltage from outputs of the current sensing circuit and the second-order slope compensation circuit.

When the power PMOS transistor turns on, a large voltage spike noise is generated at node N_{LX} as shown in Fig. 11(a). However, no spikes can be seen in V_i waveform as shown in Fig. 11(c). The V_i increases with time, accompanied by a quadratic change. When V_i exceeds V_c,

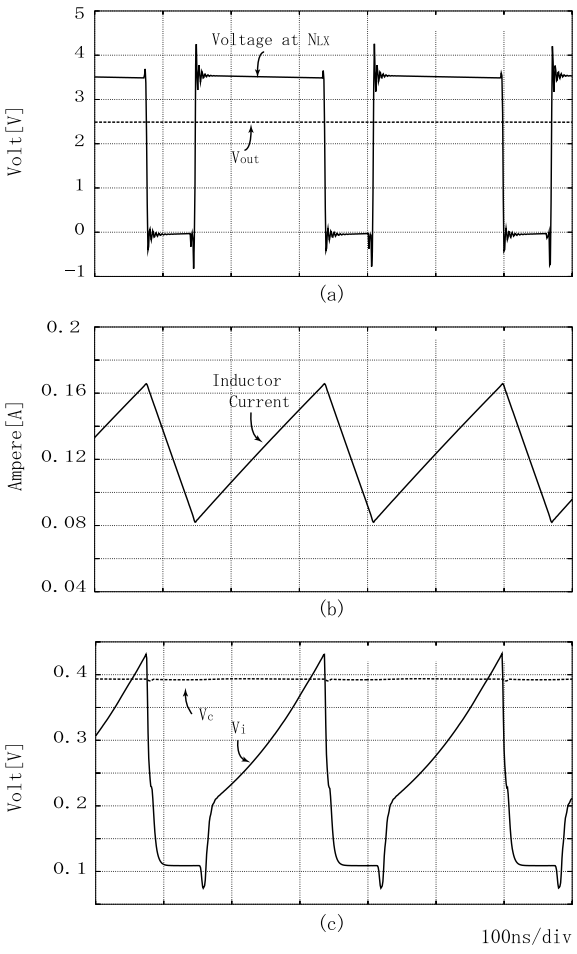

Fig. 11 The simulation result. (a) The voltage waveforms at N_{LX} and V_{out}. (b) The waveform of the current that flows through external inductor L. (c) The voltage waveforms of V_i and V_c.

the power PMOS transistor turns off and V_i is reset to bias voltage. All these figures verify the correct and stable operation.

8. Conclusion

The small signal transfer function of a PWM buck DC-DC converter with current-mode control is analyzed. We proposed the use of second-order slope compensation to avoid the output voltage dependency of the stability and the frequency bandwidth of the current feedback loop. The SPICE simulation verified the effectiveness of the method.

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