A Realization of a Below-1-V Operational and 30-MS/s Sample-and-Hold IC With a 56-dB Signal-to-Noise Ratio by Applying the Current-Based Circuit Approach

Yasuhiro Sugimoto, *Member, IEEE*

***Abstract*—This paper demonstrates the low-voltage and low-power operation of a MOS sample-and-hold circuit while preserving speed and accuracy, aiming at the realization of a pipelined low-voltage and low-power analot-to-digital converter on a system large-scale integrated circuit. It was fabricated by utilizing 0.35-μm CMOS technology. The main feature of this circuit is that all the input, signals, and output are in the current form. The circuit consists of simple current mirrors. In order to eliminate the signal-dependent current transfer ratio error, voltages at the drain terminals of mirror transistors are fixed as constant. A source degeneration resistor, which is a transistor in the triode operational region, is connected to a mirror transistor in order to alleviate the influence of the threshold and transconductance parameter variations. Control signals are boosted in voltage and applied to the gate of switch NMOS transistors in the signal path in order to reduce the on-resistance of analog switches. A differential configuration is adopted throughout the entire circuit and effectively cancels switch feedthrough errors. As a result, a 30-MS/s operation with a signal-to-noise ratio (SNR) of 56 dB from a 1-V supply has been achieved, when the input current is $\pm$200 μA. The chip even operated down to 0.85 V with a 20-MHz clock. The SNR was measured as 50 dB with an input current of $\pm$100 μA.**

***Index Terms*—0.35-μm CMOS, 0.85-V operation, 30 MS/s, 56 dB of signal-to-noise ratio (SNR), current-based circuits, sample and hold.**

I. Introduction

A LARGE-SCALE integrated (LSI) circuit's supply voltage continuously decreases. Although this supply voltage reduction is the direct consequence of device size reduction in the LSI process, it is very difficult for analog LSIs to keep up with this trend because of the reduction of dynamic range and the deterioration of signal-to-noise ratio (SNR). Among various functions, analot-to-digital converters (ADCs) and digital-to-analog converters (DACs) are major analog functions which are commonly installed together with logic functions. They are inevitably required to operate with the same supply voltage and LSI process as those of logic functions. In order to achieve the low-voltage and high-frequency operation of analog circuits, three strategies are considered. The first is the use of current rather than voltage as an information carrier [1]. The second is the suppression of voltage swing at each node even when the signal changes. The third is to boost the control voltage for an analog switch in order to reduce the on-resistance [2]. Based on these approaches, a sample-and-hold circuit is designed and fabricated using 0.35-μm CMOS technology, intending its application as the core part of the pipelined ADC.

The purpose of this paper, therefore, is to clarify whether the low-voltage operation of a sample-and-hold circuit while preserving its high-frequency and high-accuracy characteristics is realizable. In Section II, the voltage-based and current-based circuit approaches are compared in regard to the realization of a low-voltage sample-and-hold function of the ADC. Section III proposes a new circuit, which forms the core part of the designed sample-and-hold circuit, and analyzes the effect of fixing the node voltage both in dc and ac. Section IV continues to analyze the effect of the source degeneration resistor and shows its actual implementation. Section V describes the circuit design of this sample-and-hold circuit. Section VI shows the result of the chip evaluation, and Section VII concludes this study.

II. Comparison of Voltage-Based and Current-Based Approaches

In the voltage-mode pipelined ADC, an operational amplifier, capacitors, and analog switches are used to perform the sample-and-hold operation as well as the subtraction and the residue amplification in a bit-block. In sample mode, a bit-block circuit is constructed as shown in Fig. 1(a). When in hold-and-residue amplification mode, a bit-block circuit is constructed as shown in Fig. 1(b). Based on the discussion in [3], the output voltage V_o is calculated to be

$$V_o = \frac{C_s + C_f}{\left(1 + \frac{1}{A}\right) C_f + \frac{1}{A} C_s} \times V_{\text{in}}. \tag{1}$$

especially when $C_f = C_s$, (1) yields to

$$\frac{V_o}{V_{\text{in}}} \cong 2\left(1 - \frac{2}{A}\right). \tag{2}$$

In this case, a gain of 2 is ideal, and gain A should be greater than 2000 (66 dB) if we need a gain error of less than 0.1%.

Manuscript received February 3, 2003; revised September 12, 2003. This paper was recommended by Guest Editors A. Rodríguez-Vázquez, F. Mediero, and O. Feely.

The author is with the Electrical, Electronic, and Communication Engineering Department, Chuo University, Tokyo 112-8551, Japan (e-mail: sugimoto@sugi.elect.chuo-u.ac.jp).

Digital Object Identifier 10.1109/TCSI.2003.821295

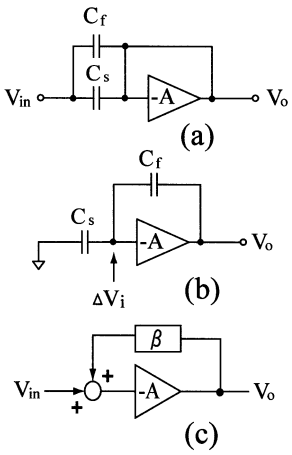

Fig. 1. Conventional sample-and-hold circuit in a pipelined ADC.

This corresponds to the allowable gain error for the first stage of a 10-b pipelined ADC.

Another constraint for the low-voltage operational op-amp is the unity gain bandwidth. The settling time of V_o in Fig. 1(b) is determined by the gain–bandwidth product of the op-amp. Fig. 1(c) shows the equivalent circuit of Fig. 1(b), where β is the feedback ratio. Suppose that the voltage gain of the op-amp has the following frequency characteristic:

$$A_{\mathrm{OL}}(s) = \frac{A_{\mathrm{OL}}(0)}{1 + s\tau_{\mathrm{OL}}} \tag{3}$$

where $1/\tau_{\mathrm{OL}}$ is the -3-dB cutoff angular frequency of the op-amp. When the step input is applied to this circuit, the output $V_o(t)$ becomes [3]

$$\frac{V_o(t)}{V_{o\ \mathrm{final}}} = 1 - e^{-(t/\tau_{\mathrm{CL}})} \tag{4}$$

where $\tau_{\mathrm{CL}} = \tau_{\mathrm{OL}}/\beta A_{\mathrm{OL}}(0)$. Provided that $A_{\mathrm{OL}}(0) \gg 1$, the condition for the output voltage error to settle within N-bit accuracy is

$$e^{-(t/\tau_{\mathrm{CL}})} \leq 2^{-N}. \tag{5}$$

As the unity gain bandwidth ω_u of the op-amp is expressed as

$$\omega_u = \frac{A_{\mathrm{OL}}(0) - 1}{\tau_{\mathrm{OL}}} \approx \frac{A_{\mathrm{OL}}(0)}{\tau_{\mathrm{OL}}} \tag{6}$$

the settling time t_{Nbit} of the circuit shown in Fig. 1(c) becomes

$$t_{\mathrm{Nbit}} \geq \frac{N \ln 2}{\beta \omega_u}. \tag{7}$$

In the case $N = 10$, $f_{\mathrm{ADC}} = 30$ MHz, that is, $t_{\mathrm{Nbit}} = 16.5$ ns, $\beta = 1/4$, we have

$$f_u \geq 267 \text{ MHz}. \tag{8}$$

This means that we need an op-amp having a gain–bandwidth product of more than 267 MHz in order to realize a 30-MS/s 10-b pipelined ADC. In the sample mode shown in Fig. 1(a), the input impedance of an op-amp increases as the input signal frequency increases due to the op-amp gain reduction. Therefore, it is more efficient for the op-amp to have higher unity gain bandwidth. Notice that these requirements for the op-amp should be realized with a supply voltage of 1 V or less. This may be a difficult requirement for voltage-based analog circuits [4].

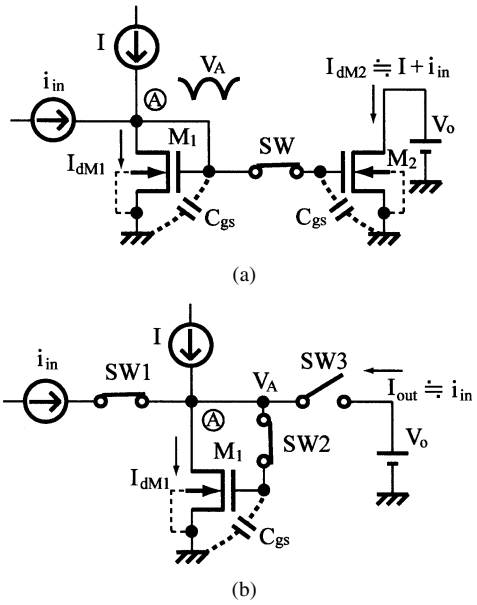

Fig. 2. Simple sample-and-hold circuit. (a) The first-generation switched-current circuit. (b) The second-generation switched-current circuit.

On the other hand, a current-based circuit is considered to have wide frequency bandwidth [5], [6]. This is because the impedance at each node is low, thus making high-frequency operation possible. Two simple current-based sample-and-hold circuits are shown in Fig. 2. Assume in Fig. 2(a) that the switch's on-resistance is zero, that transistors M_1 and M_2 are identical, and that the output voltage is fixed to the constant value V_o. For i_{in} change by steps, the time constant τ associated with the settling time at terminal A is calculated to $2C_{\mathrm{gs}}/g_m$, where g_m is the transconductance of M_1. For $C_{\mathrm{gs}} = 0.2$ pF and $g_m = 1$ mS, τ and the loop bandwidth become 0.4 ns and 400 MHz, respectively. The same kind of argument is applied for the circuit in Fig. 2(b) except that the gate capacitor is only C_{gs}.

The low-voltage operation capability of the circuit shown in Fig. 2 is rather evident. If the switch control voltage is not considered, then the minimum supply voltage becomes $V_{\mathrm{th}}+2\Delta$ for both circuits, where Δ is the minimum drain-to-source voltage necessary for a transistor to operate in a saturation operational region.

Among the circuits seen in Fig. 2, the second-generation switched-current circuit shown in Fig. 2(b) is superior to the first-generation switched-current circuit in Fig. 2(a) in that it does not suffer from device parameter mismatch because it uses the same transistor for sampling and holding the signal current. The first-generation switched-current circuit has an accuracy problem. Both circuits suffer from current transfer ratio error due to the drain-to-source voltage difference between M_1 and M_2 seen in Fig. 2(a) or between the voltage difference in sampling and in holding seen in Fig. 2(b).

Despite the above facts, we decided to use the first-generation switched-current circuit for realizing a low-voltage sample-and-hold circuit. This is because the circuit shown in

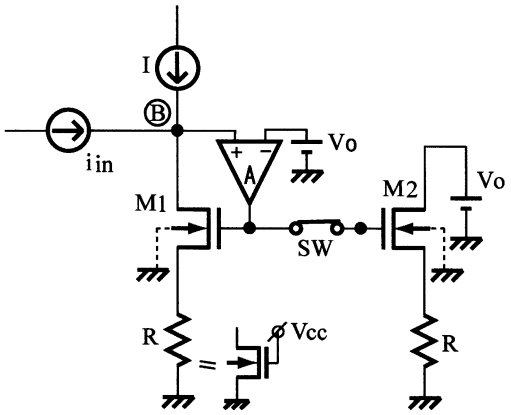

Fig. 3. A proposed sample-and-hold circuit.

Fig. 2(b) has three switches while that in Fig. 2(a) has only one. The clock feedthrough error of the circuit shown in Fig. 2(b) is larger than that of the circuit in Fig. 2(a). The amount of the clock feed-through error should be strictly controlled to obtain an accuracy of 0.2% or less. In addition to this, the short time interval when all three switches are off exists for the circuit in Fig. 2(b) in order to guarantee the nonoverlap operation of switches between SW3, SW1, and SW2. During this time interval, terminal A becomes floating and the voltage changes. This causes the injection of an additional charge into $C_{\rm gs}$ and produces a current error at the output.

III. Fixing the Node Voltage of a Current Mirror

The voltage waveform at node A (V_A) in Fig. 2(a) changes as the input current changes and, as a result, $V_{{\rm ds}M1}$ changes as shown in the figure. This means that the current transfer ratio becomes dependent on the change of input current. This causes distortion in the output current.

In order to avoid the error in the current transfer ratio and the error caused by device parameter mismatch, we propose the circuit shown in Fig. 3. The circuit in Fig. 3 uses the circuit in Fig. 2(a) with an additional low-voltage op-amp and two source resistors. The bias voltage of the op-amp is V_o and it is the same as the drain voltage of M_2. Due to the feedback operation of the op-amp, the voltage change at terminal B is suppressed even when the input signal current changes, though the voltage change across a source resistor is newly introduced. The drain-to-source voltages of transistors M_1 and M_2 now become equal and the error associated with different drain-to-source voltages is eliminated. In addition to this, it becomes possible to use a resistor between the signal source and a terminal B in order to convert the input signal voltage into the input signal current $i_{\rm in}$ when the circuit is used as an input stage of the IC.

However, questions arise as to how the op-amp is constructed under the circumstance of a low supply voltage of 1 V or less and what voltage gain and gain–bandwidth product are needed. Fig. 4 shows the small signal equivalent circuit of the one shown in Fig. 3 in sample mode, including current sources M_1, op-amp A, and resistor R_s. Because for the sake of simplicity op-amp A is assumed to have zero output impedance, it is not necessary to consider the right side of the circuit in Fig. 3.

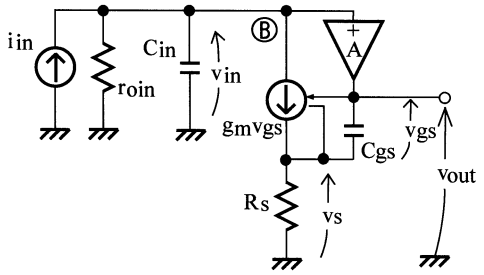

Fig. 4. Equivalent circuit for the left side of the circuit in Fig. 3.

In Fig. 4, $r_{\rm oin}$ is the combined output resistor of current sources I and $i_{\rm in}$, and the output resistance of M_1. $C_{\rm in}$ is the stray capacitor at terminal B including the drain-to-gate capacitance of M_1, $C_{\rm gs}$ and g_m are the gate-to-source capacitor and the transconductance of M_1, respectively, and $v_{\rm in}$, $v_{\rm gs}$, v_s, and $v_{\rm out}$ are signal voltages at terminal B, between the gate and source of M_1, across a resistor R_s, and at the output, respectively. The gate-to-drain capacitance of M_1 has no influence on the signal voltage at the gate of M_1 as the output impedance of op-amp A is zero.

From the figure, we obtain the transimpedance z_f as the ratio of $v_{\rm out}$ to $i_{\rm in}$ as follows:

$$z_f = \frac{v_{\rm out}}{i_{\rm in}} = \frac{(1+g_mR_s)\,Ar_{\rm oin}}{1+g_mR_s+Ag_mr_{\rm oin}} \times \frac{1+\dfrac{C_{\rm gs}R_s}{1+g_mR_s}s}{1+\dfrac{(1+g_mR_s)\,C_{\rm in}r_{\rm oin}}{1+g_mR_s+Ag_mr_{\rm oin}}s}. \tag{9}$$

Assuming that the voltage gain A of an op-amp has a first-order roll-off in frequency characteristics such that $A = A_0/(1+\tau s)$, and that s^2 term is small relative to s term and can be neglected, then (9) becomes

$$\begin{aligned} z_f &= \frac{(1+g_mR_s)\,A_0r_{\rm oin}}{1+g_mR_s+A_0g_mr_{\rm oin}} \times \frac{1+\dfrac{C_{\rm gs}R_s}{1+g_mR_s}s}{1+\dfrac{(1+g_mR_s)\,(\tau+C_{\rm in}r_{\rm oin})}{1+g_mR_s+A_0g_mr_{\rm oin}}s} \\ &\approx \left(\frac{1}{g_m}+R_s\right) \times \frac{1+\dfrac{C_{\rm gs}R_s}{1+g_mR_s}s}{1+\dfrac{2R_s(\tau+C_{\rm in}r_{\rm oin})}{A_0r_{\rm oin}}s} \end{aligned} \tag{10}$$

and $v_{\rm in}$ at terminal B becomes

$$v_{\rm in} = \frac{(1+\tau s)}{A_0}v_{\rm out} = \frac{(1+\tau s)}{A_0}z_fi_{\rm in}. \tag{11}$$

In (10) and (11), approximations such that $A_0g_mr_{\rm oin} \gg (1+g_mR_s)$ and $g_mR_s \simeq 1$ are used. For example, $g_m \simeq (1/300)$ S and $R_s \simeq 300\ \Omega$ in this design. By examining (10), the -3-dB roll-off of $v_{\rm out}$ occurs at the angular frequency

$$\omega_{-3{\rm dB}} = \frac{r_{\rm oin}}{2R_s} \times \frac{A_0}{\tau+C_{\rm in}r_{\rm oin}}. \tag{12}$$

The product $C_{\rm in}r_{\rm oin}$ may become close to τ. As A_0/τ is the unity gain bandwidth ω_t of the op-amp A, $\omega_{-3{\rm dB}}$ comes to be approximately $r_{\rm oin}\omega_t/4R_s$, and this is higher than ω_t. The maximum signal frequency that the circuit in Fig. 4 processes is only half of the sampling frequency. For the input stage circuit which converts the input signal voltage into current by using an external resistor, 2 kΩ and 300 Ω are used for $r_{\rm oin}$ and R_s, respectively. At a sampling frequency of 30 MHz, the necessary unity gain bandwidth for the op-amp is calculated to be 9 MHz.

On the other hand, the $v_{\rm in}$ at a low frequency is calculated from (11) as approximately $2R_s i_{\rm in}/A_0$. When the circuit is used in the input stage of a sample-and-hold circuit that realizes N-bit accuracy, it is necessary for $v_{\rm in}$ at terminal B to become less than 1/2 LSB of the full-scale signal input voltage $r_{\rm oin}i_{\rm in}$. Therefore,

$$\frac{2R_s i_{\rm in}}{A_0} \le 2^{-(N+1)} r_{\rm oin} i_{\rm in} \tag{13}$$

is required. This leads the criterion for A_0 and it is

$$A_0 \ge \frac{2R_s}{r_{\rm oin}2^{-(N+1)}}. \tag{14}$$

Again, with $N = 10$, $R_s = 300\ \Omega$, and $r_{\rm oin} = 2$ kΩ, the minimum value of A_0 becomes 56 dB. This value is 10 dB lower than that of the op-amp used in the voltage-based circuit shown in Fig. 1. However, (11) indicates that $v_{\rm in}$ increases as the input signal frequency increases. This means that the accuracy in voltage-to-current conversion is degraded as frequency increases. However, this kind of phenomena also happens at the inverting terminal of the op-amp seen in Fig. 1(a). As we have examined, requirements for the dc voltage gain and the unity gain bandwidth of the op-amp are greatly relaxed when the circuit shown in Fig. 3 is used instead of the circuit in Fig. 1.

IV. Effect of the Source Degeneration Resistors on Device Mismatch

The sample-and-hold circuit shown in Fig. 3 suffers from poor current mirror ratio mismatch due to device parameter mismatch such as $V_{\rm th}$ and β, where $V_{\rm th}$ is the threshold voltage of a transistor and $\beta = \mu C_{\rm ox}W/L$, μ, $C_{\rm ox}$, W, and L are mobility, unit gate capacitance, gate width, and gate length of a transistor, respectively.

The advantage of placing a resistor R at the source terminal of each current mirror transistor is that $V_{\rm th}$ and β mismatches in device parameters are suppressed. Fig. 5 shows the concept governing this. The conventional method of realizing a robust design for the $V_{\rm th}$ and β variation of a MOS current source is to use a long channel transistor, that is, a transistor with a long gate length as shown in Fig. 5(a). A long-channel MOS transistor M_{01} is considered such that it consists of two different MOS transistors M_1 and M_{11} connected in series as shown in Fig. 5(b). The lower part (M_{11}) is considered to be a source degeneration resistor because it is operated in the triode operational region as shown in Fig. 5(c). In this paper, the use of two separate MOS transistors in place of one long-channel MOS transistor is proposed as shown in Fig. 5(d). The gate terminal of a transistor M_{11} in Fig. 5(d) is connected to another supply voltage V_P which is higher than the voltage of gate V_G of M_1.

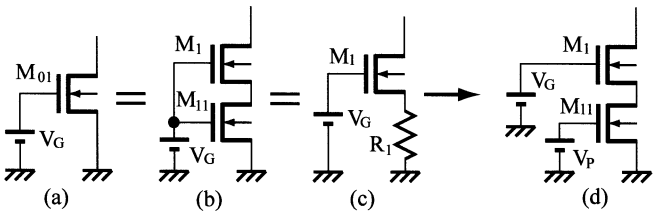

Fig. 5. Long-channel MOSFET current source and an improved current source.

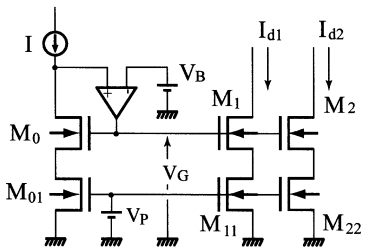

Fig. 6. Current source in which resistors are replaced by transistors in the triode operational region.

The advantage of the circuit shown in Fig. 5(d) is further examined by using the configuration as shown in Fig. 6. Now, the influence of the device parameter mismatch on currents I_{d1} and I_{d2} is analyzed. M_{01}, M_{11}, and M_{22} in Fig. 6 become the source degeneration resistors in the same manner as shown in Fig. 5(d). First, we will derive the formula for the relative error of the output current in the current mirror circuit having the source degeneration resistors.

We denote the β and $V_{\rm th}$ of transistors M_1 and M_2 as $\beta 1$, $V_{\rm th1}$, and $\beta 2$, $V_{\rm th2}$, respectively. We also denote the degeneration resistors of M_{11} and M_{22} as R_1 and R_2, respectively, and the average source voltages of M_1 and M_2 as V_s. Then, following the procedure described in [7], we obtain

$$\frac{\Delta I_d}{I_d} = \frac{-\Delta V_{{\rm th}U}}{\dfrac{V_s + g_{mU}}{2\beta_U}} + \frac{\dfrac{g_{mU}}{2\beta_U}}{\dfrac{V_s + g_{mU}}{2\beta_U}}\left(\frac{\Delta\beta_U}{\beta_U}\right) - \frac{V_s}{V_s + \dfrac{g_{mU}}{2\beta_U}}\left(\frac{\Delta R}{R}\right) \tag{15}$$

where $\beta_U = (\beta_1 + \beta_2)/2$, $\Delta\beta_U = \beta_1 - \beta_2$, $R = (R_1 + R_2)/2$, $\Delta R = R_1 - R_2$, $I_d = (I_{d1} + I_{d2})/2$, $\Delta I_d = I_{d1} - I_{d2}$, $\Delta V_{{\rm th}U} = V_{\rm th1} - V_{\rm th2}$, and $g_{mU}/\beta_U = V_{gsU} - V_{{\rm th}U}$, V_{gsU} and $V_{{\rm th}U}$ are the average gate-to-source voltage and the threshold voltage of M_1 and M_2, respectively.

The degeneration resistor is formed by using a transistor in a triode operational region as shown in Fig. 5(d). As $V_{\rm th}$ and β varies in this transistor, the resister value also varies. The relative error can be calculated as follows:

$$\frac{\Delta R}{R} = \frac{\Delta V_{{\rm th}R}}{V_P - V_{{\rm th}R}} - \left(\frac{\Delta\beta_R}{\beta_R}\right) \tag{16}$$

where $V_{{\rm th}R}$ and β_R are the $V_{\rm th}$ and β of a transistor used as a degeneration resistor.

The overall relative error is obtained by substituting (16) into (15). Now, let's take the gate area of a transistor into account

because the amount of the $V_{\rm th}$ and β variation is inversely proportional to the square root of the gate area [8]. It then becomes convenient to express the relative error by converting it to the form of standard deviation. It becomes

$$\frac{\sigma(I_d)^2}{{I_d}^2} \simeq \frac{1}{{V_s}^2 L_U W_U} \times \left\{ \sigma(V_{{\rm th}U})^2 + \left(\frac{g_{mU}}{2\beta_U}\right)^2 \left(\frac{\sigma(\beta_U)^2}{{\beta_U}^2}\right)\right\} + \frac{1}{L_R W_R}\left\{\frac{\sigma(V_{thR})^2}{(V_P - V_{{\rm th}R})^2} + \left(\frac{\sigma(\beta_R)^2}{{\beta_R}^2}\right)\right\} \quad (17)$$

where L_U, L_R, W_U, and W_R are the average gate length and the average gatewidth of transistors M_1 and M_2, and M_{11} and M_{22}, respectively.

The first term in (17) indicates that the $V_{\rm th}$ and β variation of a transistor M_1 or M_2 are suppressed by the ratio of $1/V_s$ and $g_{mU}/2\beta_U V_s$. Usually, $V_s \gg (g_{mU}/2\beta_U)$ holds. The second term in (17) also indicates that the $V_{\rm th}$ variation of a transistor used as a degeneration resistor is suppressed if V_P is greater than V_G which is the voltage used in a conventional way.

However, this comparison is not fair because the value of the degeneration resistor shown in Fig. 5(d) is smaller than that in Fig. 5(b) when $V_P \geq V_G$. In order to obtain the same degeneration resistor value, W_R in Fig. 5(d) should be set smaller than that in Fig. 5(b) by the ratio of $(V_G - V_{thR})/(V_P - V_{{\rm th}R})$. Substituting this ratio into the second term in (17) yields

$$2{\rm ndterm} = \frac{1}{L_R W_R}\left\{\frac{\sigma(V_{{\rm th}R})^2}{(V_G - V_{{\rm th}R})(V_P - V_{{\rm th}R})} + \frac{V_P - V_{{\rm th}R}}{V_G - V_{{\rm th}R}}\left(\frac{\sigma(\beta_R)^2}{{\beta_R}^2}\right)\right\}. \quad (18)$$

$V_{\rm th}$ variation is still suppressed as indicated by (18) because $V_P \geq V_G$. In this case, however, the β variation increases by the ratio of $(V_P - V_{{\rm th}R})/(V_G - V_{{\rm th}R})$. The overall error, however, still decreases because the $V_{\rm th}$ variation is dominant and is greater than the β variation.

V. Design of a Sample-and-Hold Circuit

The current-based sample-and-hold circuit was designed by using the device parameters of a 0.35-μm CMOS process. In order to reduce the clock feedthrough error and offset current, a differential configuration is adopted by using two identical channels, as shown in Fig. 7. As the difference of current between M_{c10} and M_{c13} is taken at the output, the output current value is doubled relative to the input current value. The difference signal for M_{c13} is obtained from a node in channel 2, which corresponds to terminal C in channel 1.

As for the clock feedthrough error, it does not become a problem to obtain 0.1% of linearity if the sample switch size is small (6 μm in width and 0.35 μm in length in this design), if the differential configuration is adopted to cancel out the clock feedthrough by utilizing the common mode rejection characteristic, and if a small capacitor (0.3 pF in this design) is added to the gate of the mirror transistor in order to increase capacitance that absorbs the feedthrough charge. Below -60 dB of generated harmonics was confirmed by the simulation. However, the amount of the clock feedthrough changes in this design as the input signal current changes. The source or drain voltage change of a switch transistor due to the input current change becomes opposite between channel 1 and channnel 2. As the different amount of clock feedthrough is observed there, they can't be cancelled out completely. Therefore, it is better to set the gate-to-source or -drain voltage of a switch transistor constant as proposed in [2] if less than 0.1% of linearity is necessary.

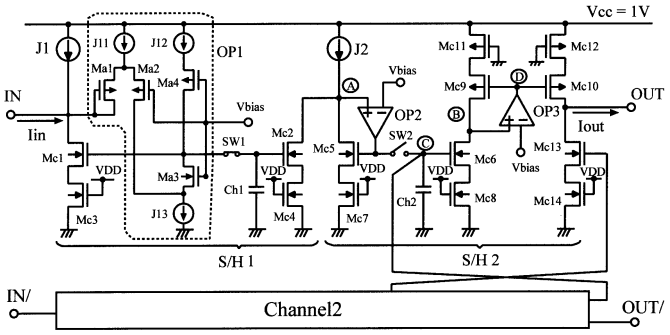

Fig. 7. Designed S/H circuit.

There are three current mirror circuits per channel, two of which have sample switches. The circuit performs double sampling. This is a provision for relaxing the slewing criteria of the circuit in a pipelined ADC because no input signal change during the one sampling period is seen. In order to further reduce the nonlinearity of the current transfer ratio in a current mirror circuit due to the small voltage variation at the drain terminals of a transistor, the direction of current increase and decrease is chosen to be opposite in these two current mirrors. That is, when the input signal current increases, the current in M_{c2} increases while the current in M_{c5} decreases. Transistors M_{c3}, M_{c4}, M_{c7}, M_{c8}, M_{c11}, M_{c12}, and M_{c14}, whose gates are connected either to the supply voltage or the ground, act as resistors.

The first-stage operational amplifier Op1 shown in Fig. 7 consists of a common-gate type transistor amplifier M_{a2} and a folded-cascode type output stage. An operational amplifier Op2 or Op3 consists of a conventional type of differential circuit. The drain terminal of M_{a1} is connected to the IN terminal and a capacitor is connected between the IN terminal and the source of M_{a3} in Op1 in order to obtain phase margin to prevent oscillation. Op2 and Op3 also have capacitors for avoiding oscillation. As an external resistor is connected to the IN terminal, the voltage gain of M_{c1} becomes low and Op1 should compensate for this. This is because the first-stage op-amp has a different configuration from the others.

This sample-and-hold circuit operates from a 1 V or less supply voltage. The source or drain voltage of a switch transistor is set around 0.5 V and the $V_{\rm th}$ is 0.35 V, and, therefore, 1 V is considered the minimum voltage for the switch control; however, the switch on-resistance becomes large. When the on-resistance increases, the high frequency characteristic deteriorates [9]. In order to reduce the on-resistance, the gate voltages of analog switches are boosted by using the circuit

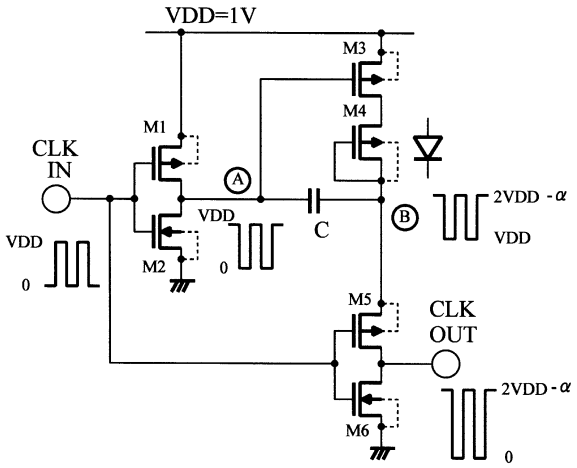

Fig. 8. Gate voltage boosting circuit.

shown in Fig. 8. The voltage is boosted by storing the charge into a capacitor and applying an offset voltage to one terminal of a capacitor. In this type of voltage-boosted circuit, the existence of any discharge path from the node under boosted voltage should be eliminated. For this purpose, a PMOS transistor M_4 with its gate and bulk terminals connected to the drain is placed between M_3 and terminal B as shown in the figure. No path including parasitic diodes exists when the voltage at terminal B becomes boosted. However, due to M_4, the boosted voltage at terminal B is slightly reduced by the amount of α, which is the threshold voltage of a PMOS transistor and is 0.3–0.35 V in this design. The boosted voltage at terminal B is used as the supply voltage for an inverter M_5 and M_6, resulting in the output voltage from 0 to $(2V_{DD} - \alpha)$. This value becomes about 1.7 V when the supply voltage is 1 V. Although the drain-to-source voltage of M_5 and M_6 becomes higher than V_{DD}, it is only 1.7 V and there occurs no reliability problem in the 0.35-μm process. The necessary control voltage for switches to keep the distortion level below -60 dB was around 1.7 V in simulation.

VI. Experimental Results

The circuit is fabricated by using 0.35-μm CMOS technology, with the $V_{\rm th}$ values of $+0.35$ V for NMOS and -0.35 V for PMOS. Fig. 9 shows a microphotograph of the chip. In the performance evaluation, the signal is applied by the voltage source and is converted to current by connecting an external resistor of 2 KΩ to the IN terminal of a sample-and-hold circuit. This sample-and-hold circuit is intended for use in the first bit-block of a current-based 10-b pipelined ADC. The output of a sample-and-hold circuit is connected to the input of the sample-and-hold circuit in the next bit-block [10]; therefore, the output voltage also becomes fixed. Only current addition and subtraction is performed in between bit-blocks.

Table I shows the measurement results of the static linearity between the input terminal and the corresponding output terminal. $I_{\rm in+}$ and $I_{\rm in-}$ are the input currents which flow into and flow back from the input terminal, respectively, while $I_{\rm out-}$ and $I_{\rm out+}$ are the output currents which flow into and flow out of the output terminal, respectively. The full-scale input is

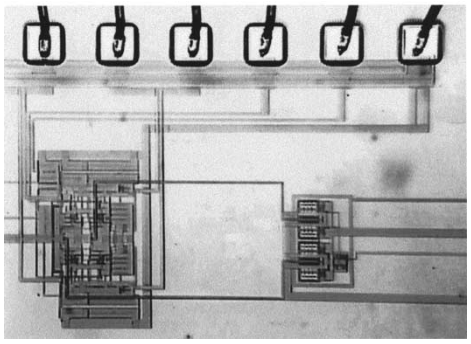

Fig. 9. Chip microphotograph of the sample-and-hold circuit.

TABLE I
Static Linearity Between the Input and Output Currents

$I_{in+} - I_{in-}$	$I_{out-} - I_{out+}$	current transfer ratio
$400\mu A$	$800.6\mu A$	2.002
$320\mu A$	$643.6\mu A$	2.011
$240\mu A$	$483.9\mu A$	2.016
$160\mu A$	$323.1\mu A$	2.019
$80\mu A$	$161.6\mu A$	2.020
$0\mu A$	$3.0\mu A$	

400 μA and the full-scale output current is 800 μA. Considering the 10-b pipelined ADC, the static linearity required for the sample-and-hold circuit in the first-stage bit-block is less than 0.2% in current transfer ratio. In this case, it should be between 2.004 and 1.996 and is calculated in Table I. In this table, the current transfer ratio seems to be shifted from the desired value 2 to 2.02. This is because the g_m of M_{c2} shown in Fig. 7 becomes slightly larger than that of M_{c1}. As the drain of M_{a1} in Op1 is connected to the IN terminal, the drain-to-source voltage of M_{a1} becomes smaller than that of M_{a2}, and this causes the voltage at IN terminal goes low (approximately 10 mV) relative to $V_{\rm bias}$. As a result, the drain-to-source voltage of M_{c1} becomes smaller than that of M_{c2}, and the current flowing through M_{c2} becomes larger than that of M_{c1}. There might be another cause from the device mismatch; however, it is not possible to analyze the effect because the number of samples is very small. The deviation, however, is limited to 0.009 in total for the 320 μA of input current change. This indicates the possibility of obtaining 10-b accuracy within this input current range. The current transfer ratio decreases when the input current range increases. The accuracy decreased to about a 9-b equivalent when the full-scale input current was applied. Though the offset is observed when the input current is zero, it is expected to be compensated for by the digital correction logic in an ADC.

Next we describe the circuit's dynamic performance. Fig. 10 shows a photograph of the input and the output waveforms. The upper waveform is a 3-MHz full-scale input signal and the lower is the output waveform. The sampling rate is 30 MS/s and V_{CC} is 1 V. The input signal is applied through a 2-kΩ resistor, while the output signal is obtained by converting output currents into voltages by using external operational amplifiers. The figure confirms the 30-MS/s and 1-V operation.

Fig. 11 shows the results of the beat frequency test with the input signal frequency close to half of the sampling frequency. The sampling rate is 30 MS/s and the input signal frequency is

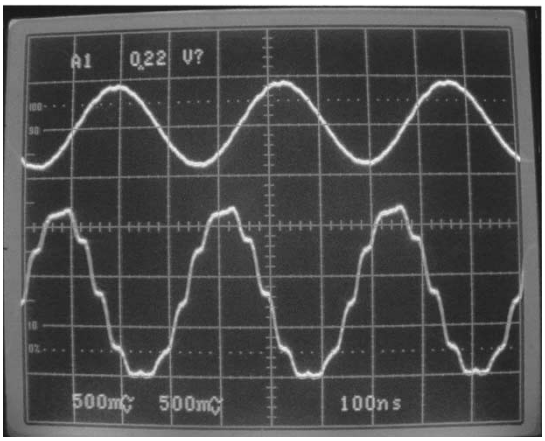

Fig. 10. Input and output waveforms (the input: 3 MHz full-scale).

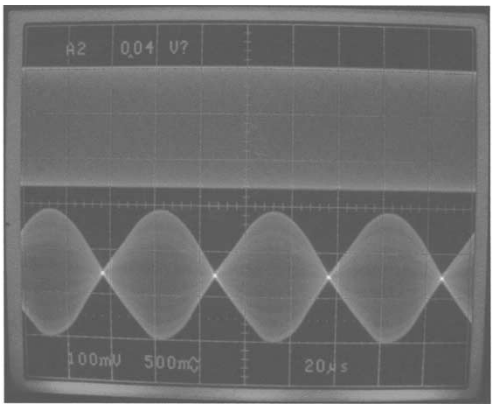

Fig. 11. Beat frequency test. (a) 14.98 MHz, −10 dB of full-scale. (b) The output waveform, $f_{\rm clock} = 30$ MHz, $V_{CC} = 1$ V).

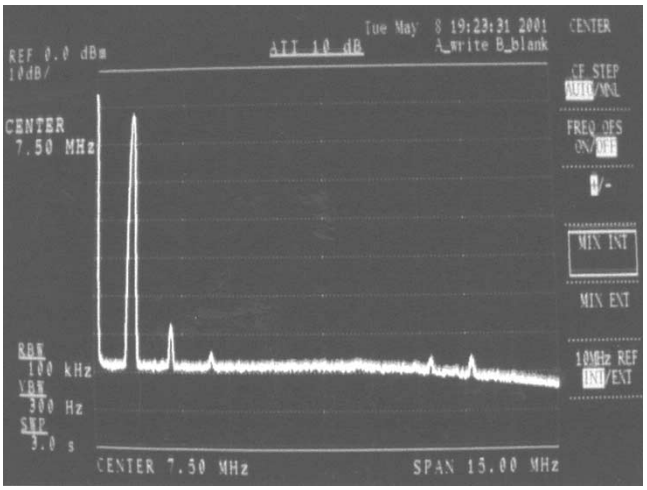

Fig. 12. Frequency spectrum of the output waveform (input: 1.32 MHz of full-scale; output: second harmonic = −55 dB of the fundamental, third harmonic = −63 dB).

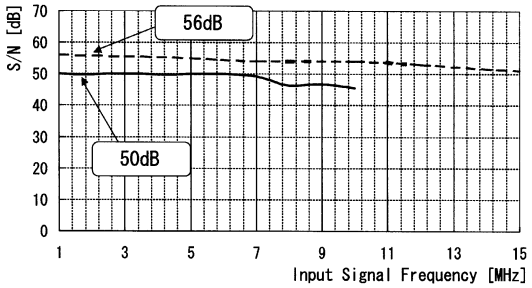

Fig. 13. Frequency characteristic of the SNR (dotted line: $V_{CC} = 1$ V; bold line: $V_{CC} = 0.85$ V).

14.98 MHz with −10 dB of the full-scale level. It is observed that the overall gain has a 3∼4-dB peak at around 15 MHz, implying a phase margin problem. In order to avoid the saturation of the signal at internal nodes, the input signal is reduced to −10 dB. The full-scale level corresponds to the input current of ±200 μA. The beat frequency test checks the slew-rate characteristic of the internal circuit because the maximum and the minimum outputs appear alternately at the vicinity of the peak amplitude. As the deterioration of the response is small, it is possible to handle the input signal up to the Nyquist frequency.

Fig. 12 shows the frequency spectrum of the output waveform. The input is −10 dB of the full-scale level with a frequency of 1.32 MHz. The sampling frequency is 30 MS/s. A 1-MHz input bandpass filter is used to effectively supress the second and third harmonics by applying a slightly shifted 1.32-MHz signal. The second and third harmonics levels of the input signal of −10 dB of the full-scale level is −63 dB and below −70 dB, respectively. Even in this setup, the harmonic level of the input signal still exceeds −60 dB when a full-scale level is applied. Therefore, the input level is reduced to −10 dB. The second and third harmonics of the output signal are measured as −55 and −63 dB in the differential configuration of the measurement setup. As the noise level is −66 dB with the 100kHz of read bandwidth when −10 dB of full-scale input is applied, the SNR is measured as 56 dB. When the sampling frequency is 20 MHz, the second harmonic becomes −58 dB. In the evaluation circuit, the output current to voltage converter is configured by external resistors, and external operational amplifiers with phase compensation capacitors. The cut-off frequency of the circuit is set approximately at 15 MHz, and the decrease in noise level shown in Fig. 12 at high frequencies accounts for this time constant.

Fig. 13 shows the SNR characteristics. The dotted line shows the SNR when the sampling frequency is 30 MHz and the supply voltage is 1 V. Even when the input signal frequency increases, the deterioration of the SNR is small up to the Nyquist frequency. The sample-and-hold circuit was operated down to 0.85 V of the supply voltage. In this case, however, the input full-scale current is reduced to ±100 μA from ±200 μA. The sampling frequency should also be reduced to 20 MS/s. Nevertheless, 50 dB of SNR is obtained and this verifies the below −1-V operation of the sample-and-hold circuit.

The sample-and-hold circuit consumes 3 mW from the 1-V power supply. This circuit adopts the double-sampling scheme and differential configuration. This increases the power consumption almost four times that of the simplest one as shown in

TABLE II
CIRCUIT'S OVERALL PERFORMANCE

Process			0.35μmCMOS $V_{thn} = +0.35V$ $V_{thp} = -0.35V$	
S/N	Vcc=1V	fin=1MHz fclk=30MHz	56	dB
		fin=15MHz fclk=30MHz	51	dB
	Vcc=0.85V	fin=1MHz fclk=20MHz	50	dB
Distortion:-10dB Input of F.S. Vcc=1V		2nd	-55	dB
		3rd	-63	dB
Power Dissipation Vcc=1V			3	mW

Fig. 3. The power can be managed when the requirement for accuracy is relaxed in the lower bit-block of an ADC. The overall performance is summarized in Table II.

VII. CONCLUSION

A 1-V or below operational, 30-MS/s sample-and-hold circuit having an SNR of 56 dB has been designed, fabricated, and evaluated by using a 0.35-μm CMOS process toward the realization of a below-1-V operational low-power pipelined ADC. In this design, a current-based circuit approach is used in order to relax the criteria posed to the dc gain and gain–bandwidth product of an operational amplifier of a voltage-based design. The chip evaluation results show that its dynamic performance is suitable for the ADC. However, the dc linearity was limited to the 9-b equivalent level. Although the source degeneration resistor scheme has been adopted to relax device mismatch, and the differential configuration is used to reduce the clock feedthrough, an improvement of dc linearity is still necessary.

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Yasuhiro Sugimoto (M'76) received the B.E. degree from the Tokyo Institute of Technology, Tokyo, Japan, in 1973, the M.E. degree from the University of Michigan, Ann Arbor, Michigan, in 1980, and the Ph.D. degree in engineering from the Tokyo Institute of Technology in 1991.

He joined Toshiba Semiconductor Group in 1973 and engaged in the development of analog VLSIs. Since 1992, he has been with the Faculty of Science and Engineering, Chuo University, Tokyo, where he is now a Professor in the Department of Electrical, Electronic, and Communication Engineering. His main interest is the design and development of new circuits in mixed-signal and RF LSIs. He is the author of three books.

Dr. Sugimoto is a Member of the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan and the Japan Consulting Engineers Association. He is the recipient of the 1989 Best Paper Award of the European Solid-State Circuits Conference and the 1998 IEICE Best Paper Award.