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PAPER

A Study of Effective Power-Reduction Methods for PDP Address-Driver ICs by Applying a Power-Dispersion Scheme

Yuji SANO[†,††a)], **Akihiro TAKAGI**[†b)], *and* **Yasuhiro SUGIMOTO**[††c)], ***Regular Members***

SUMMARY It is very difficult to simultaneously achieve power and cost reductions in address-driver circuits of a plasma-display panel (PDP) unit in which an energy-recovery scheme utilizing the resonance of a series-connected inductor and electrode parasitic capacitors is used. This is because an increase in parasitic capacitance and high-speed circuit operation become necessary as the display panel becomes larger in size and higher in resolution. In particular, low-power operation of address-driver ICs is key to avoiding the installation of heat sinks on the ICs. We propose herein new power-dispersion methods that can greatly reduce the power dissipation of address-driver ICs even when large parasitic capacitance is driven at high speed. The proposed methods enable a reduction in the power dissipation of address-driver ICs without deteriorating the operational speed by dispersing their powers into external resistors, and by supplying power to address-driver ICs in two voltage steps during both rising and falling time intervals when the address changes. Our results indicate that the power dissipation of address-driver ICs and the total cost of the address drive unit of a plasma-display panel can be reduced to 29% and 53%, respectively, compared with those of the ICs and the unit that are driven by the conventional address-driving method.

key words: *plasma display, driver circuits, driver IC, power dissipation*

1. Introduction

Plasma displays are now thought to be strong candidates for use in the near future as thin and large-size displays at home, after continuing efforts to make the screen size large, the resolution and picture quality high. However, the cost and power dissipation of current plasma displays remain high. It is therefore considered difficult to replace existing television sets such as a CRT (Cathode Ray Tube) TVs and projection TVs without the efforts to reduce the cost and power.

The cost of a plasma-display TV is almost double that of a projection TV, although prices do continue to go down. The power dissipation of a plasma-display TV ranges from 250 W to 450 W [1], while that of CRT TV and projection TV ranges from 150 W to 250 W. Cost and power dissipation are the primary obstacles to plasma-display TV becoming popular at home, despite its ability to offer a larger screen size of more than 30 inches. It is, of course, useful to reduce the power consumption of a plasma-display TV from the perspective of avoiding future energy crises. As such, for a plasma-display TV to be introduced as a popular TV set at home, it is at least necessary that the power dissipation becomes equal to that of a CRT TV of the same screen size.

There exists a strong correlation between the cost and power dissipation of a plasma-display panel. Reductions in power dissipation result in reductions in cost. Large power dissipation means large heat generation. When a reduction in power dissipation is accomplished, then some parts designed to radiate heat can be eliminated, or the size of the circuit board can be minimized, thus reducing costs. For example, the heat radiation fin attached to a driver IC and an electric fan for cooling purposes can be eliminated entirely.

An analysis of power dissipation in a PDP unit shows that a panel itself consumes 60% of the total power, with the circuits consuming the remaining 40%. The reason for the large power loss in the PDP is the low light-emitting efficiency. The light-emitting efficiency of a PDP is only 2 lm/W, while that of a CRT is approximately 5 lm/W [2]. It is considered, based on the plasma physics, that a big break through will be necessary to further reduce the power dissipation of a PDP to that of a CRT, though efforts are continuing.

A circuit's power can, however, possibly be reduced further. The address-driver circuits that drive address electrodes and activate light-emitting pixels in a PDP consume almost all of their power by driving the parasitic capacitors between electrodes. A driving method to drive half-length electrodes by splitting one long electrode into two upper-side and lower-side address electrodes in a PDP has been proposed and realized for actual panel-driving circuits [3]. This method actually doesn't use an energy-recovery scheme, though the parasitic capacitance that address-driver circuits must drive is reduced by half, thereby reducing power consumption. However, the complexity of the address-driver circuits including driver ICs is doubled, greatly

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[†]The authors are with the Fujitsu Hitachi Plasma Display Ltd., Kawasaki-shi, 213-0012 Japan.
[††]The authors are with the Department of Electrical, Electronic, and Communication Engineering, Chuo University, Tokyo, 112-8551 Japan.
a) E-mail: sano@fhp.ed.fujitsu.co.jp
b) E-mail: takagi@fhp.ed.fujitsu.co.jp
c) E-mail: sugimoto@sugi.elect.chuo-u.ac.jp

increasing the manufacturing costs.

Another method of reducing the power consumption of driver circuits that is already in use [4] is to use an energy-recovery scheme utilizing the resonance between a series-connected inductor L and the sum of electrode parasitic capacitors C. The electrostatic energy that is stored in the sum of parasitic capacitors between electrodes in the PDP, which ranges from 50–100 nF, can be recycled by using a inductor. Low-power dissipation is achieved because the stored energy is recycled instead of being dumped every time driver pulses for electrodes are generated. However, while the size and resolution of the PDP increase, the power efficiency when the energy-recovery scheme is used begins to drop, and the total power consumption becomes large. This increase in power consumption occurs because the Q-factor value of the resonance circuit becomes low due to the increase in the sum of the parasitic capacitances and the frequency of the driver signal. It is useful to reduce the number of driver electrodes per energy-recovery circuit to restore the power efficiency to its original levels. However, this reduction increases the number of energy-recovery circuits, that is, the total complexity of circuits per PDP.

As described above, it is impossible to increase the power efficiency when conventional methods are used, in that the circuit complexity increases drastically and the production costs becomes huge. As such, we propose herein a new power-reduction method that disperses the power consumption of driver ICs into an external resistor. This dispersion is realized only with a small increase in the circuit complexity. The proposed circuit can drive relatively large parasitic capacitors at high speed because the resonance of L and C is not used when the power is dispersed. In Sect. 2, conventional power-reduction methods and their related problems are described. In Sect. 3, a new power-dispersion method is proposed and analyzed. The effectiveness of connecting an external resister in series with address-driver ICs for the purpose of power dispersion, and the effectiveness of increasing or decreasing the supply voltage of address-driver ICs in two steps to reduce the total power dissipation by half are analyzed. Section 4 shows the experimental results for the proposed methods, and Sect. 5 concludes our discussion.

2. Conventional Driving Methods and Their Related Problems

Figure 1 shows the output circuit of an address-driver IC. V_a is the address drive voltage and $C_a\,(n_{IC})$ is the load capacitor at the n_{IC}th output node including parasitic capacitors between the address electrode and the ground, and between the address electrode and adjacent address electrodes. The maximum power consumption P_{d1} of the address-driver circuit is generally expressed by the following equation when the frequency of the output pulse is f.

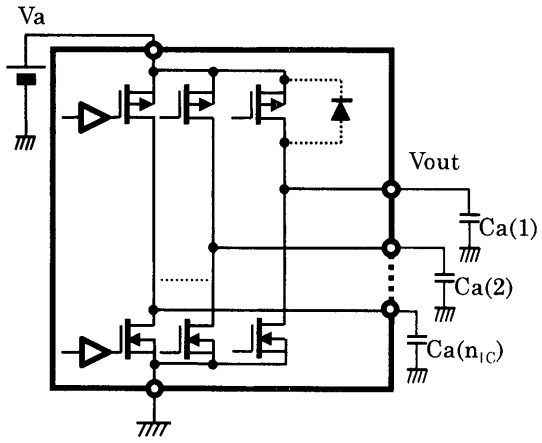

Fig. 1 Output circuit of an address-driver IC.

$$P_{d1} = nC_a f {V_a}^2 \tag{1}$$

where n shows the number of output terminals. The power dissipation reaches a maximum in the display mode when the even-numbered and odd-numbered address electrodes are alternately driven by a value between V_a and the ground. Equation (1) becomes the maximum value because the load capacitor with a parasitic capacitors is now taken into account.

2.1 A Driving Method that Uses Two Divided Address Lines

When a driving method that uses two divided address lines in the upper and lower portions of a plasma-display panel is used, the load capacitor value C_a becomes one-half that of the one without division. As the number of pixels that each address electrode should drive is also halved, the frequency f of the output pulse can also be reduced by half. As a result, the maximum power dissipation per address-driver IC (P_{d2}) becomes one-fourth the power dissipation of the conventional driving method (P_{d1}). When the power dissipation of the IC is decreased, the problems associated with heat generation are lessened. Elimination of heat sinks from driver ICs simplifies the circuit board for the plasma-display panel. The circuit complexity, however, is almost doubled, making the circuit board more complicated. As such, the manufacturing cost does not change significantly.

2.2 A Driving Method Using the Energy-Recovery Scheme

Figure 2 shows the address-driver circuit that adopts the energy-recovery scheme. Power dissipation can be reduced without increasing circuit complexity by adopting the energy-recovery scheme. The following is a step-by-step explanation for circuit operation by

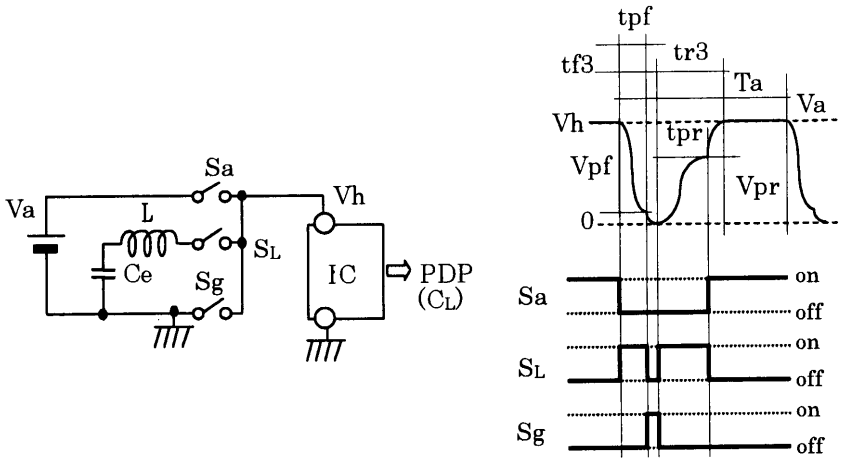

Fig. 2 Address-driver circuit in which the energy-recovery scheme is used.

utilizing the waveform of the supply terminal voltage V_h of an address-driver IC. The address-driver IC enters into the reset mode when the switch S_a, through which the address drive voltage V_a is supplied, is turned off. At the same time, switch S_L is turned on while switch S_g is still turned off. This produces the LC resonance between the inductor L and the sum of load capacitors C_L during the time interval of t_{pf} shown in Fig. 2. As one of the terminal voltage of the inductor L is kept to $V_a/2$ by a large value of capacitor C_e, the supply terminal voltage V_h of the address-driver IC starts to decrease toward the ground level. In a short time, the switch S_L is turned off when the supply terminal voltage V_h reaches its minimum after decreasing the amount by V_{pf} in the resonance process. The load capacitors are also discharged in this interval through the address-driver IC. The power dissipation that occurs during this discharge process, however, is minimized by the energy transfer scheme which utilizes the LC resonance. After that, the switch S_g is turned on and pulls down the supply terminal voltage V_h to become the ground. The outputs of the address-driver IC are switched to prepare for the next addressing control cycle in the PDP panel during this time interval when the supply terminal voltage V_h is at the ground level. The power dissipation consumed by this switching operation is also minimized because the voltage at each part of the IC is in ground level. After switching the outputs of the address-driver IC, the switch S_L is turned on and the supply terminal voltage V_h increases by utilizing the LC resonance without consuming a significant amount of energy. After the time interval of t_{pr} when the supply terminal voltage V_h reaches its maximum V_{pr} due to the LC resonance, the switch S_L is turned off. The switch S_a is then turned on and pulls up the supply terminal voltage V_h to V_a. The above operation is repeated at every time interval of T_a, which is the address-driving interval, and results in the power reduction in the address-driver circuit.

Next, the power dissipation of this method that adopts the energy-recovery scheme is calculated. A load capacitor C_a at each output terminal, which includes parasitic capacitors between adjacent address electrodes, is maximized during the operation of the alternate driving of the adjacent address electrodes from the V_a voltage level to the ground level and vice versa. Under this condition, the power dissipation reaches a maximum. For this reason, the analysis is carried out by assuming that the sum of load capacitors C_L is equal to $nC_a/2$. The maximum power dissipation of the address-driver IC (P_{d3}) is calculated as follows,

$$P_{d3} = P_{drr} + P_{drf} + P_{dsr} + P_{dsf} \tag{2}$$

where P_{drr} is the power dissipation of an address-driver IC during the rising interval of the supply terminal voltage V_h from the ground to V_{pr}, and P_{drf} is that during the falling interval of the supply terminal voltage V_h from V_a to $V_a - V_{pf}$, under the condition that resonance is established. P_{dsr} is the power dissipation necessary to force the supply terminal voltage V_{pr} to V_a, and P_{dsf} is that necessary to force the supply terminal voltage $V_a - V_{pf}$ to the ground, after the resonance operation. The on-resistances of the switches shown in Fig. 2 are chosen to be sufficiently small compared with the on-resistances of the PMOS transistor R_r and the parasitic diode R_d shown in Fig. 1. Therefore, the on-resistances of these switches can be ignored in the following analyses.

Defining the natural angular frequency and the damping factor of the LC resonance during the rising interval of the supply terminal voltage as ω_r and σ_r, respectively, then, i_{rr} which flows into the high-side PMOS transistor in the address-driver IC, is expressed as [5],

$$i_{rr} = \frac{V_a \exp(-\sigma_r t) \sin(\omega_r t)}{2L\omega_r} \tag{3}$$

Then, P_{drr} becomes,

$$P_{drr} = nfR_r \int_0^{tpr} irr^2 dt = nfR_r \int_0^{\pi/\omega_r} \left\{ \frac{V_a \exp(-\sigma_r t)\sin(\omega_r t)}{2L\omega_r} \right\}^2 dt = \frac{nfV_a{}^2 \{1 - \exp(-2\pi\sigma_r/\omega_r)\}}{8L(\omega_r{}^2 + \sigma_r{}^2)} \quad (4)$$

where

$$\omega_r = \sqrt{\omega_0{}^2 - \sigma_r{}^2}, \omega_0 = \sqrt{2/nLC_a}, \sigma_r = R_r/nL.$$

On the other hand, the voltage V_{pr} which the supply terminal voltage V_h of the address-driver IC approaches in the LC resonance process is expressed as,

$$V_{pr} = \frac{V_a \{1 + \exp(-\pi\sigma_r/\omega_r)\}}{2} \quad (5)$$

by citing the equation in Ref. [5].

Then, P_{dsr}, which is the power dissipation when the supply terminal voltage V_h is pulled up from V_{pr} to the address drive voltage V_a, is calculated as,

$$P_{dsr} = \frac{nfC_a(V_a - V_{pr})^2}{2} = \frac{nfC_a}{2}\left[V_a - \frac{V_a}{2}\left\{1 + \exp\left(\frac{-\pi\sigma_r}{\omega_r}\right)\right\}\right]^2 = \frac{nfC_aV_a{}^2}{8}\left\{1 - \exp\left(\frac{-\pi\sigma_r}{\omega_r}\right)\right\}^2 \quad (6)$$

The power dissipations P_{drf} and P_{dsf} are analyzed in the same manner when the supply terminal voltage V_h of the address-driver IC decreases. Finally, the maximum power dissipation P_{d3} of the address-driver IC in Eq. (2) becomes,

$$P_{d3} = \frac{nfV_a{}^2}{8} \times \left[\frac{2}{nL}\left\{\frac{1 - \exp\left(\frac{-2\pi\sigma_r}{\omega_r}\right)}{\omega_r{}^2 + \sigma_r{}^2} + \frac{1 - \exp\left(\frac{-2\pi\sigma_f}{\omega_f}\right)}{\omega_f{}^2 + \sigma_f{}^2}\right\} + C_a\left\{\left(1 - \exp\left(\frac{-\pi\sigma_r}{\omega_r}\right)\right)^2 + \left(1 - \exp\left(\frac{-\pi\sigma_f}{\omega_f}\right)\right)^2\right\}\right] \quad (7)$$

where, $\omega_f = \sqrt{\omega_0{}^2 - \sigma_f{}^2}$, $\sigma_f = R_d/nL$.

In contrast, the transient time $tf3 + tr3$ shown in Fig. 2 is the sum of time of LC resonance and switching after resonance, and is expressed as [5],

$$tf3 + tr3 = \frac{\pi}{\omega_r} + \frac{\pi}{\omega_f} + C_a(R_r + R_d)\ln\left(\frac{1}{1 - k_{CR}}\right) \quad (8)$$

The first two terms in Eq. (8) show the time necessary for the resonance operation, and the third term is the sum of the response time for the supply terminal voltage V_h of the address-driver IC to reach the address drive voltage V_a and to reach the ground level after the resonance operation. The third term is the response time of the CR circuit, and is measured by calculating the k_{CR} times of the voltage difference between the initial value of V_h immediately after the resonance operation to its final value, starting from the initial value. Here, k_{CR} is chosen as 0.9. During the transient time, as expressed in Eq. (8), the voltage of the address electrodes is unstable. We found it necessary to limit the transient time to within 400 ns, which is less than 30% of the address drive interval T_a by the actual measurement, so as to drive the address electrode at high speed. Assuming the following condition, for example, P_{d3} in Eq. (7) is reduced to only 10.3% of P_{d1} in Eq. (1) and $tf3 + tr3$ is shortened to 300 ns: (C_a : 66.5 pF, R_r : 190 Ω, R_d : 12 Ω, V_a : 60 V, n : 128, L : 426 nH).

The transient time $tf3+tr3$ increases in proportion to the root of nL, as implied in Eq. (8). However, it is difficult to lower the inductance L in a resonance circuit beyond the parasitic inductance of routing wires. On a printed circuit board, for example, the typical wire inductance is approximately 200 nH, meaning that the number of output terminals that one energy-recovery circuit can drive is limited due to the parasitic inductance of the routing wires. Considering the drive of a large high resolution PDP such as the one for HDTV, the maximum number of output terminals n per energy-recovery circuit is calculated as approximately 270 by Eq. (8) under the condition of having at least 200 nH of parasitic inductance and less than 400 ns of $tf3 + tr3$. The PDP panel has more than 3000 terminals as address electrodes, and, therefore, more than 10 energy-recovery circuits are needed. It is difficult to realize this kind of PDP unit from a manufacturing-cost perspective.

3. Power-Dispersion Methods

3.1 Connecting a Resistor in Series with the Power Supplies of Address-Driver ICs

A power-dispersion method that involves connecting a resistor R_{vh} in series with the power supplies of address-driver ICs, as shown in Fig. 3, is proposed in order to reduce the power dissipation of address-driver ICs and to realize low-cost driver circuits. Commonly, the resistor R_{vh} is shared with several driver ICs; however, for explanation purposes only one IC is drawn in Fig. 3. The power is dispersed to an external resistor in proportion to the resistance ratio between the on-resistance of the driver transistor in the IC and an external resistor. The heat generation of the IC is suppressed, and man-

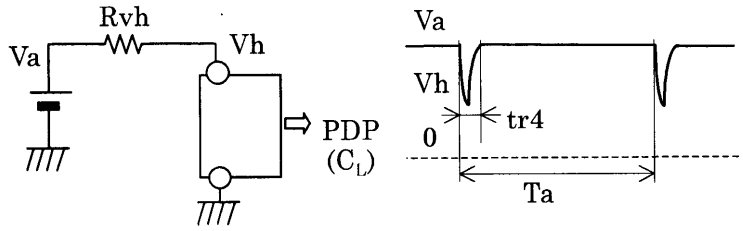

Fig. 3 Address-driver circuit using a power-dispersion technique utilizing an external resistor.

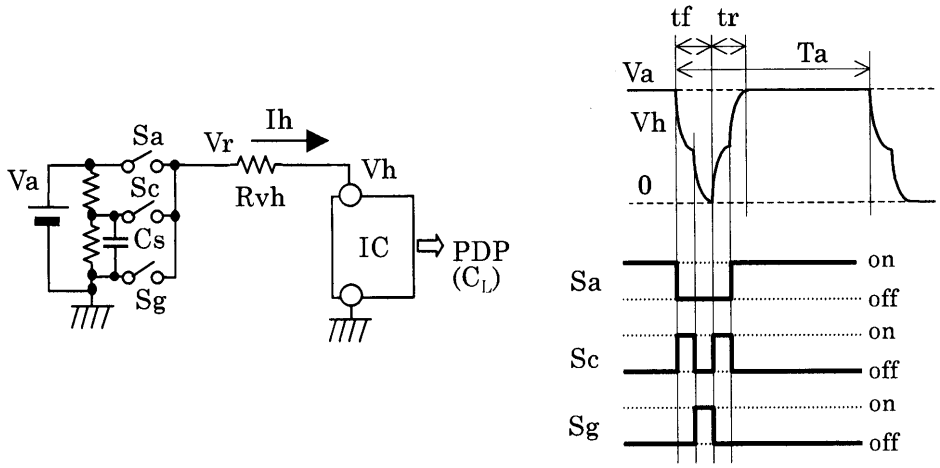

Fig. 4 Address-driver circuit using power-dispersion techniques utilizing a power-dispersion resistor and changing the supply voltage in two steps.

ufacturing costs are reduced because of the reduction of the heat sink and its installation. The voltage drop across the resistor R_{vh} occurs only when the current flows in the output PMOS transistor at the high side of the address-driver IC during the rising interval of the output voltage as can be seen in the waveform of the supply terminal voltage V_h shown in Fig. 3. Therefore, the transient time $tr4$ is approximately given by the time necessary for the output of the address-driver IC to rise from the ground level, and is calculated as,

$$tr4 \approx C_a \left(R_r + \frac{nR_{vh}}{2} \right) \ln \left(\frac{1}{1 - k_{CR}} \right) \tag{9}$$

The $tr4$ is determined by the CR time-constant multiplied by the coefficient, which is in logarithmic form. The coefficient is the response time ratio when the output of the address-driver IC starts rising from the ground level to the voltage value which is k_{CR} times the final voltage value. The k_{CR} value is again 0.9. The maximum power dissipation P_{d4} of all the address-driver ICs becomes,

$$P_{d4} = nC_a f {V_a}^2 \left\{ 1 - \frac{k_{SW4}}{2\left(1 + \frac{2R_r}{nR_{vh}}\right)} \right\} \tag{10}$$

where the switching coefficient k_{SW4} is the increasing ratio between the actual power dissipation and the power dissipation that is derived analytically by assuming the on-resistance of the drive transistor constant. The former is larger than the latter, since the on-resistance of the drive transistor decreases and approaches the on-resistance at DC during the turn-on interval of the switch, step by step, and the effective on-resistance is large. In our experiment, k_{SW4} is chosen to be 2.7. However, P_{d4}, which is calculated by Eq. (10), is only 0.71 times the P_{d1}, where the P_{d1} is the power dissipation when no power-saving method is adopted, under the same driving condition. This means that the power-reduction effect is small. Here, n is chosen to be 256, which is the number of output terminals in the IC module, and R_{vh} is chosen to be 5.3 Ω. As the power-reduction effect is quite small, the heat-radiation structure cannot be simplified to a significant extent.

3.2 A Method for Changing the Supply Voltage Step-by-Step

In order to further reduce the power dissipation of the driver IC, the power-dispersion method shown in Fig. 4 is proposed. For explanation purposes, only one IC is drawn. In Fig. 4, in addition to a resistor R_{vh}, there are resistors that divide V_a, a capacitor C_s that becomes the equivalent $V_a/2$ voltage source, and switch circuits of S_a, S_c, and S_g that switch the voltages of the supply of the address-driver IC. By repeating the operation

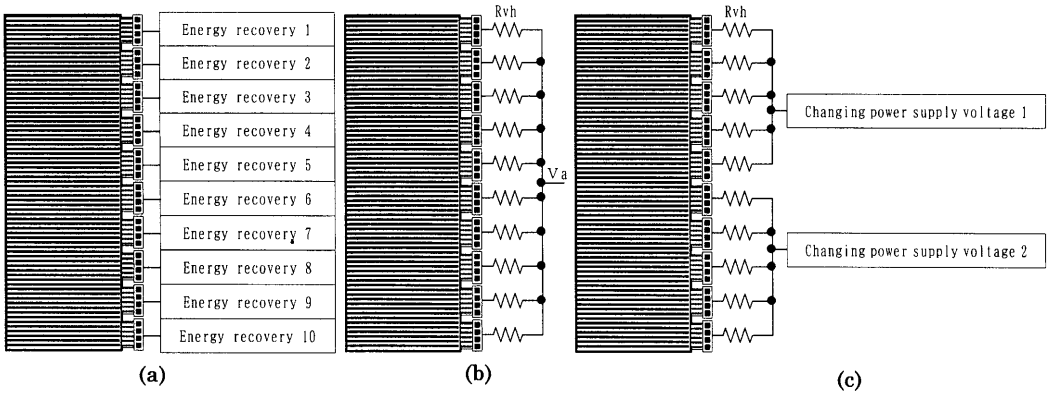

Fig. 5 Driver circuit structure for three types of address-driving methods. (a) Energy-recovery method; (b) Power-dispersion method with a series resistor; (C) Power-dispersion method using a two-step control of the IC supply voltage and having a series resistor.

such that the supply terminal voltage V_h of the address-driver IC decreases in several steps, IC outputs are then switched, and the supply voltage is increased in several steps again, thus reducing the total power dissipation. When the N equal steps are used to change the supply voltage, the power dissipation is expected to be reduced to $1/N$ [6]. A two-step change in supply voltage was used in this experiment, which involves a trade-off between circuit complexity and drive speed. The terminal voltage at which a switch S_c and a large capacitor C_s are connected, therefore, is kept at $V_a/2$. The maximum power dissipation P_{d5} of all the address-driver ICs is calculated as,

$$P_{d5} = \frac{nC_a f k_{SW4} {V_a}^2}{4} \left(\frac{1}{1 + \frac{nR_{vh}}{2R_r}} + \frac{1}{1 + \frac{nR_{vh}}{2R_d}} \right) \quad (11)$$

The terms in brackets in Eq. (11) shows the divided ratio of the on-resistance of the drive transistor in the IC and a resistor R_{vh} in the output current path. The first term is used to account for the rising edge at the output of the address drive IC, and the second term is to account for the falling edge. The power dispersion is considered in proportion to the divided ratio. The multiplication term shows the power dissipation of all the drive circuits. The calculated value of P_{d5} in Eq. (11) is only 0.16 times the power dissipation of P_{d1}. A relatively large power-reduction effect is expected.

The transient time $tf5 + tr5$ shown in Fig. 4 is calculated as follows:

$$tf5 + tr5 = 2C_a k_{PEAK} (R_r + R_d + nR_{vh}) \ln \left(\frac{1}{1 - k_{CR}} \right) \quad (12)$$

The peaking coefficient k_{PEAK} shows the shortcut-time ratio associated with the parallel peaking effect due to resonance between the wire's parasitic inductance and the load capacitor C_a. According to the calculation using Eq. (12), $tf5 + tr5$ becomes less than 400 ns, which is negligible compared with the address-drive interval T_a, if the k_{PEAK} value can be set to less than 0.63. When the wire parasitic inductance is more than 120 nH, the k_{PEAK} value decreases to 0.50 [7], and $tf5 + tr5$ becomes less than 300 ns.

4. Experimental Results

The measurement set-up of the address-driver circuits is shown in Fig. 5. In this experiment, a PDP with 852 pixels in a horizontal line and with 42 inches of diagonal length is used. The number of driving electrodes is 2556. As discussed earlier, the number of address electrodes that one energy-recovery circuit in Fig. 5(a) can drive is limited to 256, which is driven by using 4 ICs, due to the existence of the parasitic wire inductance. This means that 10 energy-recovery circuits are needed to drive one panel. The capacitor value of C_e in the energy-recovery circuit shown in Fig. 2 is chosen to be 0.1 μF, which is sufficiently larger than the maximum load capacitor value of C_L which is the sum of capacitances of the half of the 256 addreess electrodes. In the driver circuit that uses the power-dispersion method by an external resistor in series with the IC power supplies, the power dissipation of the address-driver IC is reduced when the resistor value is high and the number of driving electrodes is as small as possible. For this reason, a resistor value R_{vh} is chosen to be 5.30 Ω for every 256 outputs of the IC module, as shown in Fig. 5(b). The address-driver circuit that adopts the power-dispersion method by controlling the IC supply voltages in two steps in addition to connecting an external resistor in series with the IC power supplies, drives 1278 electrodes by way of 20 address-driver ICs. There are only two driver circuits, as shown in Fig. 5(C). The capacitor value of C_s seen in Fig. 4 is chosen to be 1 μF, which is sufficiently larger than the maximum load capacitor value of C_L which is the sum of capacitances of half of the 1278 addreess electrodes. At the same time, the power dissipation is dispersed by using a resistor

R_{vh} of 5.30 Ω for every 256 outputs of the IC module.

The voltage waveform for the power-dispersion circuit shown in Fig. 5(b) is shown in Fig. 6. The transient times for both rising and falling intervals are limited to less than 300 ns. The voltage and current waveforms at each node for the power-dispersion method described in Fig. 4, in which the power-supply voltage of the ICs is given in two steps together with the use of a power-dispersion resistor R_{vh}, are shown in Fig. 7. It can be seen that two peaks appear in the current waveform I_h because the supply terminal voltage V_h of the address-driver IC is controlled in two steps. An overshoot has appeared in the waveform of the supply terminal voltage V_h of the address-driver IC, which is produced by the parasitic wire inductances.

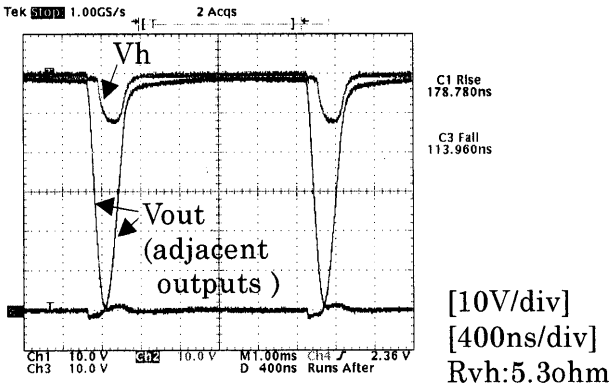

Fig. 6 Voltage waveforms of the circuit shown in Fig. 3.

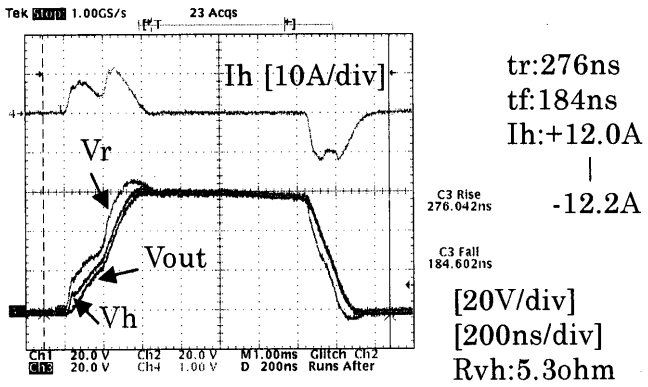

Fig. 7 Current and voltage waveforms of the circuit shown in Fig. 4.

A comparison among various power-reduction methods for the address-driver circuit is tabulated in Table 1. The energy-recovery scheme can reduce the power dissipation of the address-driver IC to one-fourth; however, it can reduce the parts cost to only 80%. In contrast, for the power-dispersion method, in which the power-supply voltage of ICs is given in two steps together with the use of a power-dispersion resistor R_{vh}, can reduce the power dissipation of the address-driver IC to 29% and the parts cost to approximately half that of the conventional driving method. This reduction can be achieved because 20 address-driver ICs can be driven by one drive circuit. Experimentally, however, the power dissipation was not reduced by half when the power-supply voltage of ICs is given in two steps, as in the ideal case. This increase in power dissipation from the ideal value stems from the through-current in switches when the power supplies of the address-driver ICs are switched. We believe that a further reduction in the power dissipation is possible if the circuits are integrated on a chip so that they can operate stably at high-speed. The present experimental results were obtained by using a setup involving discrete transistors. We were also able to clarify from the experiment that the power reduction of the power-dispersion method having a resistor in series with the power supply of the IC is only 15%. This result is due to the power being dispersed only during the rising interval of the IC output waveform. As such, the number of parts required for heat radiation cannot be reduced much in the IC module, and the reduction in parts costs remains at only 30%.

5. Conclusion

Power dispersion methods for address-driver circuits

Table 1 Comparison of the various power-reduction methods.

Power reduction method		No reduction	Energy recovery	Power dispersion	
				Use a resistor	Supply control
No. of driver ICs per one driver circuit		No	4	4	20
No. of power reduction circuit per one pannel		No	10	10	2
Power Consumption	Total (W)	18.2	8.9	17.8	14.2
	Driver IC (W/4ICs) (Ratio)	14.3 (100%)	3.5 (24%)	12.2 (85%)	4.2 (29%)
Material cost per IC pinout (Ratio)		100%	80%	67%	53%

are newly proposed for a large, high-resolution PDP that reduce the power dissipation of the address-driver IC and enable high-speed operation. The proposed circuit uses methods in which the power-supply voltage of ICs is driven in two steps together with the use of a power-dispersion resistor. Experimental results indicate that the power dissipation of the address-driver ICs becomes 29% and the parts cost becomes 53% that of conventional methods by applying the proposed method. The cost of address-driver circuits in the current plasma-display TV is one-fourth the total cost. By applying the proposed method, we would like to further promote the popular use of plasma displays at home.

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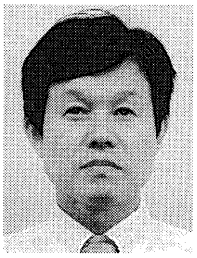
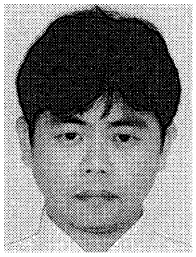
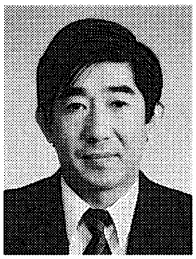


Yuji Sano received the B.E. degree and M.E. degree from Tokyo University of Science, Chiba, Japan, in 1983 and 1985 respectively. He joined Hitachi Ltd. in 1985, and engaged in the development of CRT Displays. Since 1999 he has been assigned to Fujitsu Hitachi Plasma Display Ltd. where he is now engaged in the development of Plasma Displays. His main interest is the design and development of new circuits. He was awarded a paper announcement prize from the Institute of Electrical Engineers of Japan in 1993. He is a member of the Society for Information Display, the Institute of Image Information and Television Engineers, and the Institute of Electrical Engineers of Japan.



Akihiro Takagi received the B.E. degree and M.E. degree from Tokai University, Kanagawa, Japan, in 1994 and 1996 respectively. He joined Fujitsu Ltd. in 1996, and engaged in the development of Plasma Displays. Since 1999 he has been assigned to Fujitsu Hitachi Plasma Display Ltd. His main interest is the design and development of new circuits and driving methods for PDP.



Yasuhiro Sugimoto received the B.E. degree from Tokyo Institute of Technology, Tokyo, Japan, M.E. degree from University of Michigan, Ann Arbor, Michigan, and Doctor of Engineering degree from Tokyo Institute of Technology, Tokyo, Japan, in 1973, 1980, and 1991, respectively. He joined Toshiba Semiconductor Group in 1973, and has engaged in the development of analog VLSIs. Since 1992 he has been with the Faculty of Science and Engineering, Chuo University where he is now a professor in the Department of Electrical, Electronic, and Communication Engineering. His main interest is the design and development of new circuits in mixed-signal and RF LSIs. He is the receipant of the 1989 Best Papers Award of the European Solid-State Circuits Conference and the 1998 IEICE Best Papers Award. He is the author of three books. Dr. Sugimoto is a member of the Institute of Electrical and Electronics Engineers, INC., the Institute of Electrical Engineers of Japan, and the Japan Consulting Engineers Association.