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Low-Power and Low-Voltage Analog Circuit Techniques towards the 1 V Operation of Baseband and RF LSIs

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SUMMARY This paper describes low-power and low-voltage analog circuit techniques applicable to deep sub-micron LSIs in baseband and RF signal processing. The trends indicate that reductions in the supply voltage are inevitable, that power dissipation will not become sufficiently low, and that performance will improve continuously. Some circuit techniques currently being used to achieve these goals are reviewed. Next, three trial approaches are introduced. The first of these is a 1 V operational video-speed CMOS sample-and-hold IC. The second is a 1 V operational high-frequency CMOS VCO circuit. Finally, a step-down DC-DC converter IC with a 1 V output and a greater than 80% power efficiency is introduced. These approaches prove that the low-power and low-voltage operation of analog circuits can be realized without sacrificing performance.

key words: *low-power and low-voltage analog, sample-and-hold, VCO, DC-DC converter, 1 V operation*

1. Introduction

The driving force behind the realization of low-power LSIs is apparently the popularization of mobile devices. Since these devices are battery-operated, the power consumption of LSIs is critical to their operation time. To achieve the goal of low power consumption and complex functionality, the devices in LSIs have been reduced in size every year. By maintaining a constant electric field in a transistor, low-power and high-speed characteristics with high packing density have been realized by compromising the supply voltage [1], [2]. This trade-off is in fact preferable for logic circuits, because it allows ever-higher speed and packing density without the need to increase power.

However, analog circuits must handle signals with multi-level voltages. Some voltages must be allocated to voltage swing. However, a system on-a-chip design and the ability to operate on the same supply voltage as the logic circuits do are strongly required in analog circuits these days. This indicates that we have to achieve the low-voltage operation of analog circuits whether we like or not. Because lowering the supply voltage reduces the dynamic range, the preservation of the performance is a concern. It can be easily imagined that the currents flowing through transistors can't be reduced much to preserve the frequency characteristics. In this paper, we demonstrate that lowering the supply voltage and the power consumption without diminishing performance is possible. In Sect. 2, the trends in analog LSIs, such as analog-to-digital converters (ADCs) and voltage controlled oscillators (VCOs) are reviewed. Section 3 investigates current circuit techniques to achieve low-power and low-voltage operation. Sections 4, 5 and 6 introduce our approach to a 1 V operational video-rate low-power sample-and-hold (S/H), a 1 V operational low-power high-frequency VCO, and a DC-DC converter with a 1 V output.

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2. Some Trends in Analog Circuits

Figure 1 shows the SIA's year-by-year forecast of the design rule changes and the supply voltage changes in analog CMOS LSIs. According to the forecast, the design rule and the supply voltage of CMOS analog LSIs are getting smaller every year. This is due mainly to the device size reduction in LSIs. Since reliability suffers at higher voltages, LSIs are forced to operate at lower voltages. Among the many analog functions, high-speed ADCs are some of the most important. Figure 2 plots the accuracy and supply voltage of some high-speed CMOS ADCs presented at several international conferences. As the figure shows, the accuracy has been increasing every year, while the supply voltage has been decreasing. Although an ADC with 14-bit resolution has recently been developped, the supply voltage has not been reduced enough for it to be installed on a 1 V operational future system LSI [3]. However, the

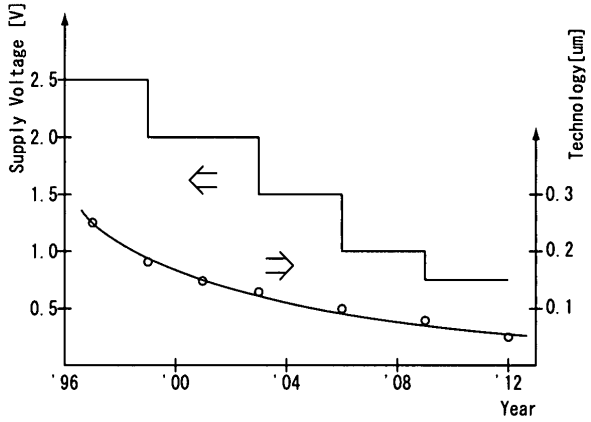

Fig. 1 Forcast of the design rule change and the supply voltage change (from SIA).

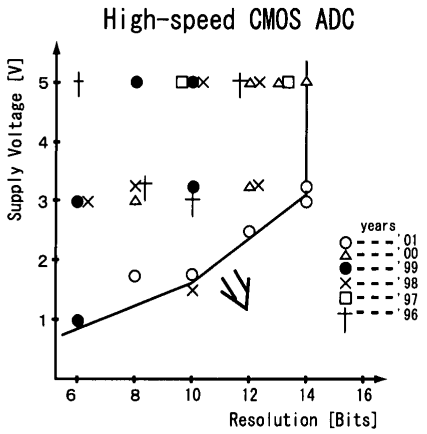

Fig. 2 The accuracy and supply voltage of high-speed CMOS ADCs.

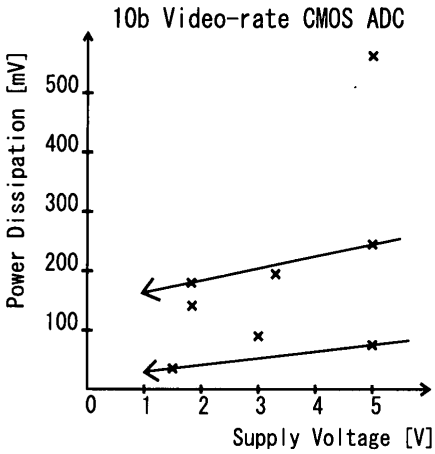

Fig. 3 The supply voltage and power dissipation of 10-b video-rate CMOS ADCs.

1 V operation of a 6-bit ADC has also been reported [4]. Figure 3 plots the supply voltage and power dissipation of recently-developped 10-bit video-rate CMOS ADCs. As the supply voltage decreases, so does the power dissipation. However, the power reduction is surprizingly small. Therefore, it may be difficult to reduce the power dissipation in analog LSIs, even when the power supply is significantly reduced. Figure 4 plots the supply voltage and power dissipation of 1.8 GHz CMOS VCOs. On the whole, both the power dissipation and supply voltage have been decreasing. But it is not apparent that the products operated by the lower supply voltage have lower power dissipation. The performance improvement of CMOS VCOs is clearly seen in Fig. 5. This figure plots the oscilation frequency and phase noise of these VCOs. On the whole, the oscillation frequency has been increasing, while the phase noise has been decreasing.

The trends illustrated in Figs. 2 to 5 indicate that the supply voltage is reduced and the performance is increased in analog LSIs as the device size is reduced. Power dissipation is also decreasing, though not by much.

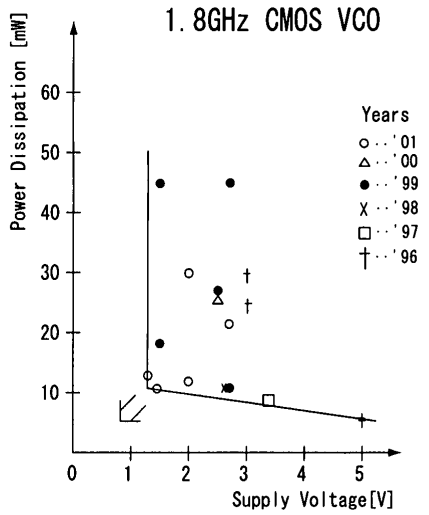

Fig. 4 The supply voltage and power dissipation of 1.8 GHz CMOS VCOs.

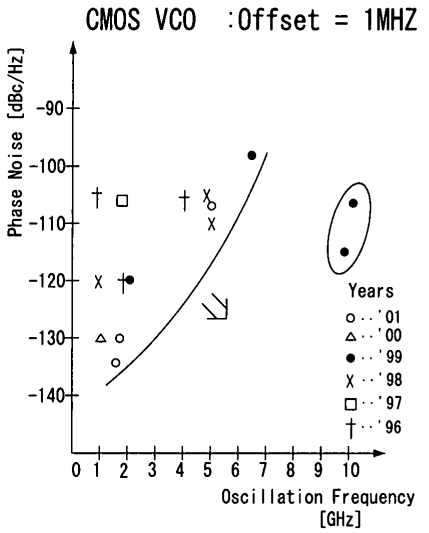

Fig. 5 The oscillation frequency and the phase noise of high-frequency CMOS VCOs.

3. Some Recent Low-Power and Low-Voltage Circuit Techniques

In this section, we briefly review current circuit techniques that provide low-power and low-voltage operation.

Analog switches are used frequently in CMOS analog circuits. However, the performance of the analog switch deteriorates as the supply voltage falls. Figure 6 shows the circuit and the on-resistance characteristic of an analog switch. Usually, the input is the signal, and the output is the load capacitor. As the input voltage level changes along with changes in the signal, the analog switch turns off when the V_{in} becomes more than $V_{DD} - V_{th}$, where V_{th} is the threshold voltage of a transistor. When V_{DD} is reduced, the voltage range at which the switch is on decreases, as shown in the figure. When V_{DD} becomes very low, such as 1 V, the analog

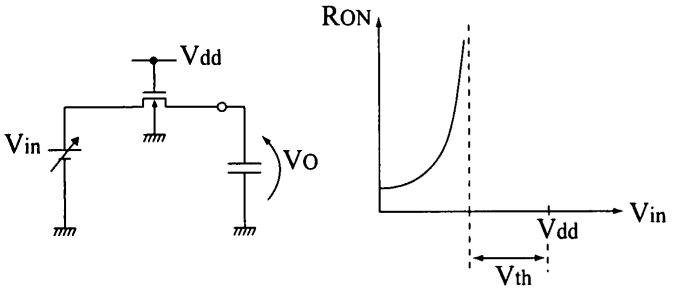

Fig. 6 Analog switch and its performance.

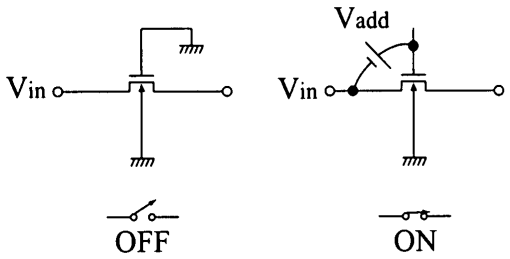

Fig. 7 Gate voltage boosting technique.

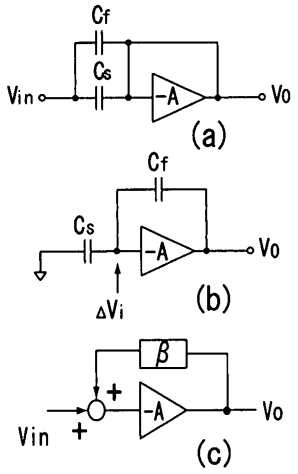

Fig. 8 The bit-block circuit in the pipelined ADC.

switch becomes hard to turn on throughout most of the input signal. In order to avoid this situation, the gate voltage of an analog switch is boosted above the V_{DD} level, as shown in Fig. 7. The switch turns off when the gate is connected to the ground, and turns on with little on-resistance when a voltage higher than V_{DD} is applied. If the boosted voltage is applied between the gate and the source and is constant, then the signal dependency for the on-resistance is completely eliminated. A circuit that produces constant voltage between the gate and the source terminals has been developped [5].

When the supply voltage approaches 1 V, how can we realize a high-gain and high-speed operational amplifier? In the pipelined ADC, an operational amplifier, capacitors, and analog switches are used to perform the sample-and-hold operation as well as the residue amplification in a bit-block. In the sample mode, a bit-block circuit is constructed as shown in Fig. 8(a). For simplicity, we assume the dc level of the input and the output is equal to the ground. Let Q be the total charge stored in capacitors C_s and C_f. When in hold and residue amplication mode, a bit-block circuit is constructed as shown in Fig. 8(b). Let Q' be the total charge of capacitors and ΔV_i be the voltage change at the inverting input of an op-amp.

Then, the following holds,

$$\begin{aligned} Q &= (C_s + C_f)\, V_{in} \\ Q' &= -C_s \Delta V_i + C_f\,(V_o - \Delta V_i) \\ V_o &= -A \Delta V_i \\ Q &= Q' \end{aligned} \tag{1}$$

From Eq. (1), the output voltage V_o is calculated to be,

$$V_o = \frac{C_s + C_f}{\left(1 + \frac{1}{A}\right) C_f + \frac{1}{A} C_s} \times V_{in} \tag{2}$$

Especially when $C_f = C_s$, Eq. (2) yeilds to,

$$\frac{V_o}{V_{in}} \cong 2\left(1 - \frac{2}{A}\right) \tag{3}$$

Equation (3) indicates that the gain V_o/V_{in} is affected by the open-loop gain of the op-amp. In this case, the gain of 2 is ideal, and the gain A should be greater than 2000 (66 dB) if we need a gain error of less than 0.1%. This corresponds to the allowable gain error for the first stage of a 10-bit pipelined ADC.

Another constraint for the low-voltage op-amp is the gain-bandwidth. Figure 8(c) is the equivalent circuit of Fig. 8(b), where β is the feedback ratio. The settling time of V_o in Fig. 8(b) is determined by the gain-bandwidth of the op-amp. Suppose that the voltage gain of the op-amp has the following frequency characteristic,

$$A_{OL}(s) = \frac{A_{OL}(0)}{1 + s\tau_{OL}} \tag{4}$$

Then, the closed loop gain of the circuit in Fig. 8(c) becomes,

$$\begin{aligned} A_{CL}(s) &= \frac{-A_{OL}(s)}{1 + \beta A_{OL}(s)} \\ &= \frac{-1}{\beta(1 + s\tau_{CL})} \end{aligned} \tag{5}$$

provided that $A_{OL}(0) \gg 1$, and $\tau_{CL} = \tau_{OL}/\beta A_{OL}(0)$. When the step input is applied to this circuit, the output $V_o(s)$ becomes,

$$V_o(s) = A_{CL}(s) \times \frac{1}{s} \tag{6}$$

and the Inverse Laplace Transformation yeilds

$$\frac{V_o(t)}{V_{ofinal}} = 1 - e^{-\frac{t}{\tau_{CL}}} \tag{7}$$

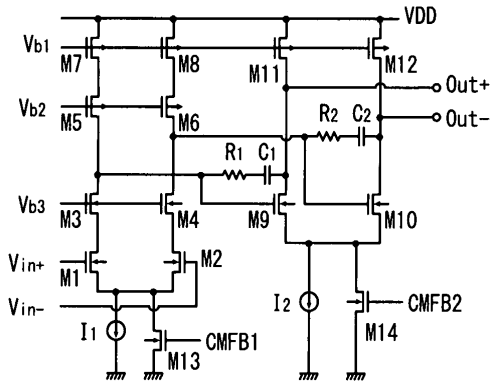

Fig. 9 Two-stage operational amplifier.

The condition for the output voltage error to settle within Nbit accuracy is,

$$e^{-\frac{t}{\tau_{CL}}} \leq 2^{-N} \tag{8}$$

that is,

$$t_{Nbit} \geq N \ln 2 \times \tau_{CL} \tag{9}$$

As the unity gain bandwidth ω_u of the op-amp is expressed as,

$$\omega_u = \frac{A_{OL}(0) - 1}{\tau_{OL}} \approx \frac{A_{OL}(0)}{\tau_{OL}} \tag{10}$$

the settling time t_{Nbit} of the circuit in Fig. 8(c) becomes,

$$t_{Nbit} \geq \frac{N \ln 2}{\beta \omega_u} \tag{11}$$

In the case $N = 10$ bit, $f_{ADC} = 20$ MHz, $\beta = 1/4$, we have,

$$f_u \geq 178\,\text{MHz} \tag{12}$$

In order to realize the 10-bit ADC, we need an op-amp with a gain-bandwidth of more than 178 MHz and with a low-frequency gain of more than 66 dB. In addition, this should be realized with a supply voltage of 1 V. To satisfy these tough requirements, a op-amp circuit that cascades the differential amplifiers, as shown in Fig. 9, has been developped [6]. As the signal is amplified in two stages, the low-frequency voltage gain becomes large. However, the phase margin is always lost in this type of amplifier. A method to move the zero into infinity [7] is adopted in order to keep the phase margin large. Reference [6] says that the low-frequency gain exceeding 100 dB and the gain-bandwidth product of 1 GHz were obtained by using 0.18 μm CMOS technology. However, the supply voltage was limmited to 1.8 V. Further efforts are needed to achieve lower voltage operation.

In high frequency circuits such as the low noise amplifier (LNA), VCO, and RF power amplifier, passive components such as inductors and capacitors are used.

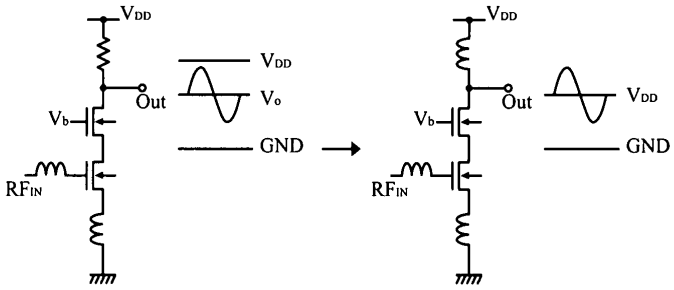

Fig. 10 LNA circuit using inductors.

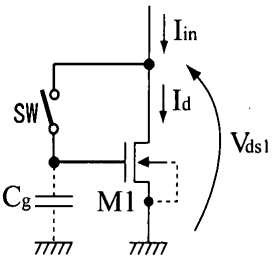

Fig. 11 A current switch circuit.

As the signal frequency is very high (several GHz), the values of these components are small. Figure 10 shows the advantage of the inductor over a conventional circuit in LNA when the supply voltage is low [8]. Inductors at the gate and source of an input transistor achieve impedance and noise-maching. Inductors at the drain of the output transistors are loads. As the inductor is the energy storage device, the output terminal can deviate to more than V_{DD}. This greatly helps the circuit to operate with a low supply voltage, as shown in Fig. 10. A capacitor is used to connect the output signal to the next stage input. A capacitor cuts the DC voltage, and the bias in the next stage can be chosen arbitrarily. Passive components in RF circuits are very useful, although the performance is relatively poor when these circuits are made on a silicon die.

Another circuit technique to realize low-power and low-voltage operation is the use of a current-based circuit. In this approach, the current value instead of the voltage value is processed. The simple current-mirror becomes the basic function. Figure 11 shows the circuit that realizes the sample-and-hold function in a current-based circuit. When the swich is turned on (sample mode), I_{in} flows through a transistor M1 and the gate-to-source voltage is memorized onto C_g. When the switch is turned off (hold mode), the gate-to-source voltage of M1 remains constant, and the constant current flows through a transistor. In this way, the sample-and-hold operation is performed. In the sample mode, the transistor M1 act as a resistor. The settling time of the V_{ds}, when a transistor changes from the hold mode to the sample mode, is related to the -3 dB bandwidth of a circuit, and it becomes [9],

$$f_c = \frac{3\mu_n(V_{gs1} - V_{th1})}{4\pi {L_1}^2} \quad (13)$$

where V_{th1} is the threshold voltage, μ_n is the mobility, and L_1 is the channel length of M1. Substituting $L_1 = 0.5\,\mu$m, $V_{gs1} - V_{th1} = 0.3$ V and $\mu_n = 550\,\text{cm}^2/\text{Vs}$, $f_c \approx 15$ GHz is obtained. As each node in the current based circuit is low-impedance, it has a superior high-frequency characteristic. The problem is accuracy in a current-based circuit, because the current mirror ratio is not good, as it suffers from parameter mismatches and drain-to-source voltage differences of mirror transistors.

4. A 1 V CMOS S/H IC with 56 dB of S/N at 30 MS/s

In order to acertain the possibility of low voltage operation, a 1 V CMOS S/H IC with a 56 dB of S/N at 30 MS/s is introduced [10]. The current-based circuit approach is used throughout the design because it helps reduce both the supply voltage and the power consumption. A current gain of 2 is selected, aiming at use in a pipelined ADC. Figure 12 shows the conceptual circuit. A current-mirror circuit, consisting of M1 and M2, is used to transfer the input current to the output. An MOS analog switch, which is inserted in between the current-mirror transistors, performs the sample-and-hold operation. When this switch is turned on, a simple current-mirror circuit is formed. When it is turned off, the gate-to-source voltage of M2 is memorized in a hold capacitor, and the current in M2 is kept constant. As IN and OUT terminals can be set at 0.5 V, the 1 V operation of the circuit becomes possible. As the frequency characteristic of a current-mirror is good, as indicated in Eq. (13), we can reduce the circuit current in signal paths. However, a S/H circuit using a conventional current-mirror circuit has an accuracy problem. The four major causes of accuracy degradation are the signal-dependent drain-to-source voltage change, the g_m change, the device parameter mismatch, and the clock feed-through. In order to improve the accuracy, op-amps are added, as shown in the figure.

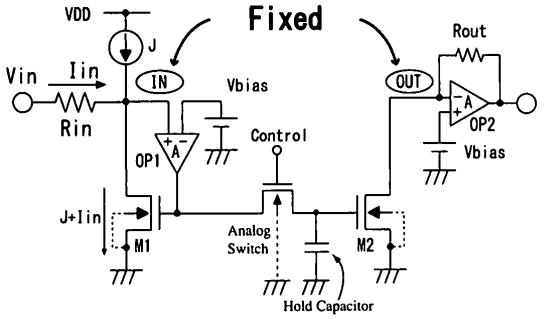

Fig. 12 Current-mirror-based S/H circuit with fixed IN and OUT terminals.

The overall S/H circuit is shown in Fig. 13. To avoid the influence of the device parameter mismatch, transistors equivalent to resistors are connected to the sources of mirror transistors. Transistors Mc3, Mc4, Mc7, Mc8, Mc11, Mc12 and Mc14, whose gates are connected to either the supply voltage or the ground, act as resistors. To reduce the on-resistance, the gate voltages of analog switches are boosted to the constant value of 1.7 V in the case of $V_{DD} = 1$ V. We need not be concerned about keeping the drain-to-source voltage constant. The circuit is differentially configured so that the even harmonics can be reduced. The circuit performs double sampling. As the difference between the current in channel 1 and the current in channel 2 is taken at the output, the output current value is doubled relative to the input current value. In order to avoid clock feed-through error, it is preferable to minimize the number of analog switches in the signal paths. Among the different types of current-mirror circuits, two are candidates to become S/H circuits. One is shown in Fig. 11, and the other in Fig. 12. The circuit in Fig. 11 needs at least two analog switches, and the drain volt-

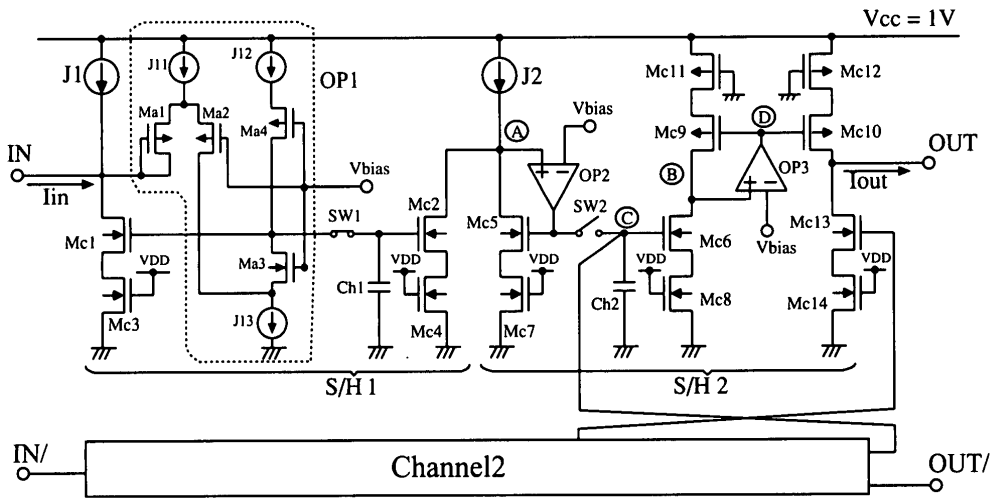

Fig. 13 Overall S/H circuit.

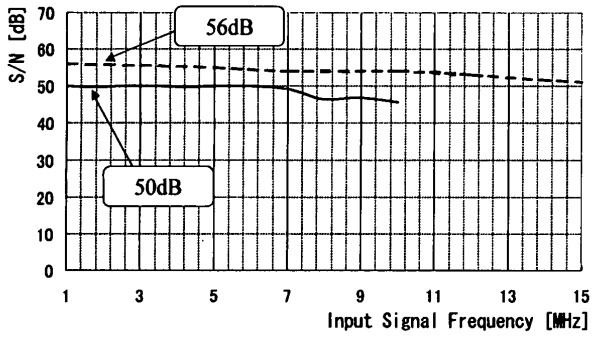

Fig. 14 Input signal frequency vs. signal-to-noise ratio.
dotted: $f_{clock} = 30\,\text{MHz}$, $V_{cc} = 1\,\text{V}$, $I_{in} = \pm 200\,\mu\text{A}$
bold: $f_{clock} = 20\,\text{MHz}$, $V_{cc} = 0.85\,\text{V}$, $I_{in} = \pm 100\,\mu\text{A}$

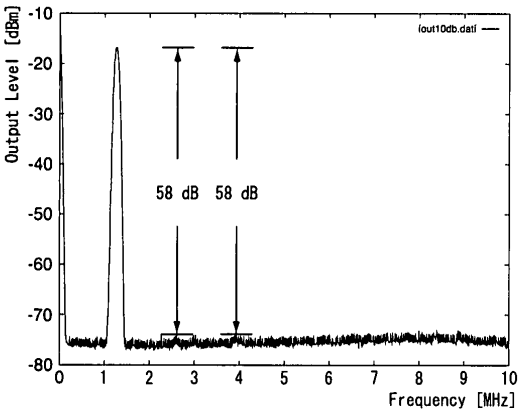

Fig. 15 Distortion characteristic (full-scale input).

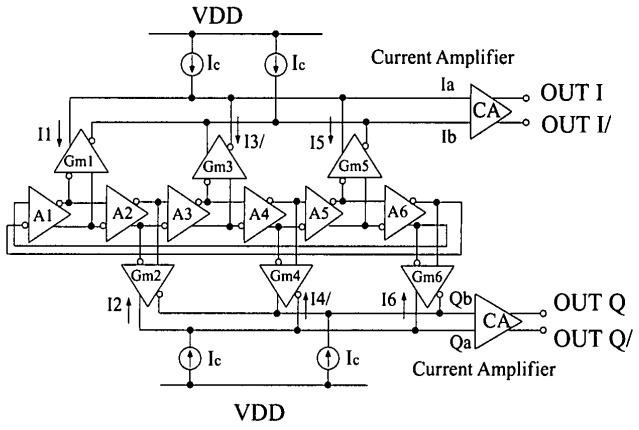

Fig. 16 Block diagram of the designed VCO.

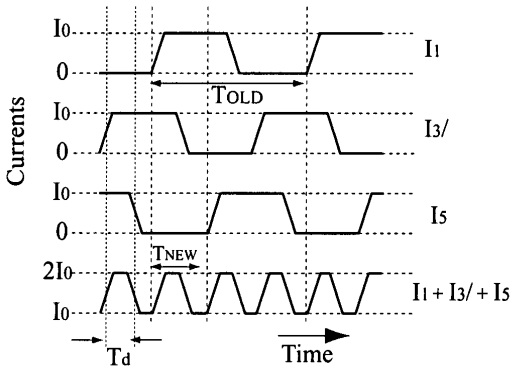

Fig. 17 Timing diagram of each current.

age of M1 begins to float when the two switches change their states, since a non-overlapping operation is required. This injects spike noise into the signal path and deteriorates the accuracy. Therefore, we decided to use the circuit in Fig. 12. It never causes floating at any drain nodes, and has only one switch transistor. However, it is necessary to be careful of parameter mismatch in this type of circuit. To further minimize the influence of clock feed-through error, the differential configuration is adopted throughout the circuit, as shown in Fig. 13.

The circuit is fabricated by using $0.35\,\mu$m CMOS technology, with the V_{th} values of $+0.35\,\text{V}$ for NMOS and $-0.35\,\text{V}$ for PMOS. The frequency characteristic of the signal-to-noise ratio (S/N) is shown in Fig. 14. The IC operates down to 0.85 V for the supply. The dotted line shows S/N with a 1 V supply at a 30 MHz clock over the frequency range of the input signal from 1 MHz to 15 MHz. Putting only one resistor between the signal source and the IN terminal in Fig. 13 can produce a non-distorted input full-scale current of $\pm 200\,\mu\text{A}$. This is because the voltage at the IN terminal is fixed. Even when the supply voltage is reduced to 0.85 V, the IC still works, and 50 dB of S/N is obtained. In this case, the input full-scale current is reduced to $\pm 100\,\mu\text{A}$ and the clock frequency to 20 MHz.

As only 60 dB of dynamic range was required, we were not concerned with the signal-dependent on-resistance change of the switch, because it is low enough when the gate voltage is boosted. Figure 15 verifies this. For a 1.32 MHz input with a 1 V supply and a 20 MHz clock, the 2nd and 3rd harmonics levels were each 58 dB, and therefore there was no need to consider signal dependent on-resistance variation. The power dissipation of this chip was 3 mW in total from a 1 V supply voltage. As this S/H circuit is assumed to be used in the first bit-block of a pipelined ADC, the S/Hs in other bit-blocks can be simplified and low-powered.

5. A Low-Voltage and High-Frequency VCO Circuit with I and Q Outputs

A high-frequency VCO circuit was designed [11]. Figure 16 shows the block diagram. Six differential inverters form a ring oscillator whose oscillation frequency is one-third of the VCO output frequency. The power dissipation of the ring oscillator could be minimized because the oscillation frequency slows. In order to multiply the ring oscillator frequency to the VCO output frequency, three signals at outputs of every second inverters are combined into one by using the current switching cells (g_m cells). The g_m cell consists of a current source I_s and a pair of current switches, which are controlled by the outputs of the delay cells.

Figure 17 shows how the ring oscillator frequency

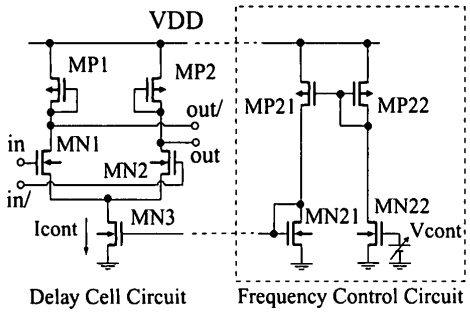

Fig. 18 Delay cell and frequency control circuits.

is multiplied. By summing up currents from g_m cells I_1, $I_3/$ and I_5, the current $I_1 + I_3/ + I_5$, which toggles between I_o to $2I_o$ at a speed three times faster than the ring oscillator frequency, is obtained. The difference of the current between I_c and $I_1 + I_3/ + I_5$ flows into the current amplifier and is amplified. By providing two multiply circuits, VCO outputs that are 90 degrees apart in phase with each other are obtained (I and Q outputs). Figure 18 shows the delay cell and the frequency control circuits. The differential delay cell consists of differential amplifiers MN1 and MN2, load transistors MP1 and MP2, and a variable current source MN3. The delay cell current I_{cont} is controlled by the V_{cont} and becomes,

$$I_{cont} = \frac{\beta_N}{2}(V_{cont} - V_{th})^2 \times K \tag{14}$$

where K is the overall current-mirror ratio from MP22 to MN3, β_N is the transconductance parameter, and V_{th} is the threshold voltage of MN22. The equivalent resistor R_{Leq} of a load resistor is,

$$R_{Leq} = \frac{1}{g_m} = \frac{1}{\sqrt{2\beta_P I_{cont}}} \tag{15}$$

where, β_P is the transconductance parameter of MP1 and MP2. Then, the time delay t_{dcell} of a delay cell becomes,

$$t_{dcell} = R_{Leq} C_L \ln 2 \tag{16}$$

where, C_L is the load capacitance at the output of a delay cell. The oscillation frequency f_{osc} of a ring oscillator with six inverter cells is,

$$f_{osc} = \frac{1}{12 t_{dcell}} \tag{17}$$

A linear relationship between f_{osc} and V_{cont} is obtained. However, the current amplifier (CA in Fig. 16) is needed because the output current of the multiply circuit is small. The current amplifier consumes a lot of power, and effective current buffering is necessary. The circuit in Fig. 18 can operate down to $V_{th} + \Delta$, where Δ is the voltage to maintain a MOS transistor in saturation, and it becomes possible to operate from the 1 V supply voltage.

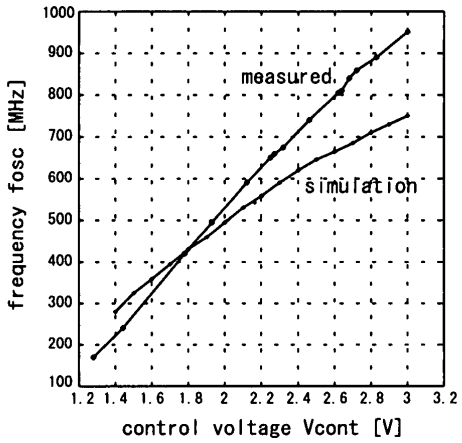

Fig. 19 Control voltage vs. oscillation frequency.

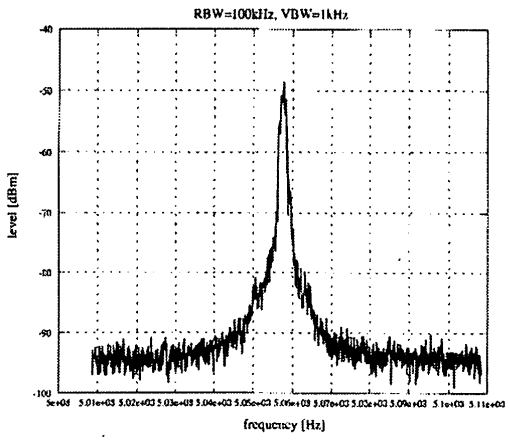

Fig. 20 Frequency spectrum at the VCO output.

The circuit was fabricated by using 0.6 μm CMOS technology. Figure 19 shows the frequency control characteristic. Because we made mistakes in layout design, the chip didn't work with a supply voltage of less than 2 V. I_{cont} was far smaller than we had designed it to be. Even under this poor condition, the linear frequency control characteristic was observed. When $V_{DD} = V_{cont} = 2$ V, the oscillation frequency was 500 MHz.

Figure 20 shows the frequency spectrum at the VCO output. The power dissipation was 11 mW in total, including the output buffers. The phase noise was only -90 dBc/Hz with a 1 MHz offset. However, the 2 V operation was confirmed, and the frequency control characteristic agreed with the circuit simulation. Therefore, we can conclude that the design is applicable to realize a low-voltage, low-power, and high-frequency VCO.

6. A 1 MHz, Synchronous Step-Down DC-DC Converter with a 1 V Output

A step-down voltage converter from 3.6 V to 1 V with a power efficiency of more than 80% is introduced [12].

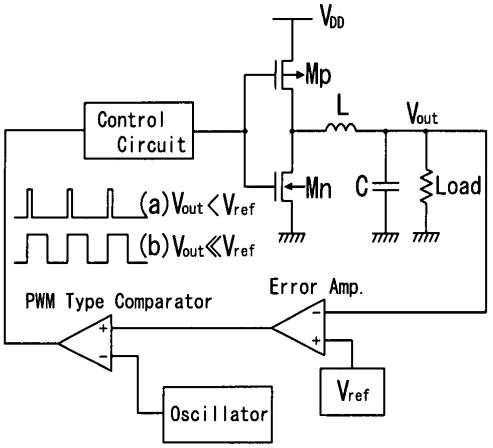

Fig. 21 PWM control scheme.

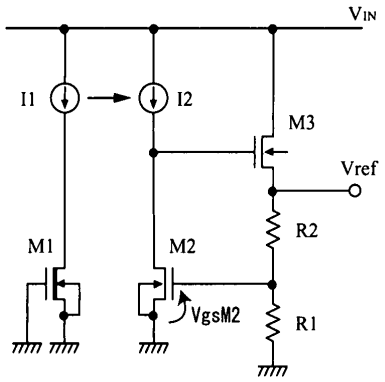

Fig. 22 1.0 V voltage reference.

The block diagram of the developed DC-DC converter is shown in Fig. 21. The L, C, and load resistor are external. The 1 MHz operation makes the external inductance and capacitance values low. The output voltage is controlled to 1 V by a PWM waveform whose time interval is fixed to 1 μs. The harmonics at the output appear at the fixed frequencies because a fixed time interval was used. This suppresses the undesirable noise interference in a system. In order to realize the 1 V output, the output devices must be MOS transistors (Mp and Mn in Fig. 21). However, this causes the problem of reverse current flow. When the load is light, the energy stored in an external coil L is quickly released. This occurs halfway through a fixed time interval, and when Mn is on. Mn continues to turn on until the end of the fixed time interval. The energy stored in an external C then begins to release, resulting in a reverse current flow. This causes the undesirable energy dissipation.

Now the output is 1 V, and a supply- and temperature-independent 1 V reference is needed so that the output voltage doesn't change at any time. The circuit shown in Fig. 22 realizes a 1.0 V reference. The depletion-mode transistor M1 is used. It becomes a voltage-independent current source when the gate terminal is connected to the ground. Then, I_1 is,

$$I_1 = \frac{\beta_1}{2}(0 - V_{thd})^2 \tag{18}$$

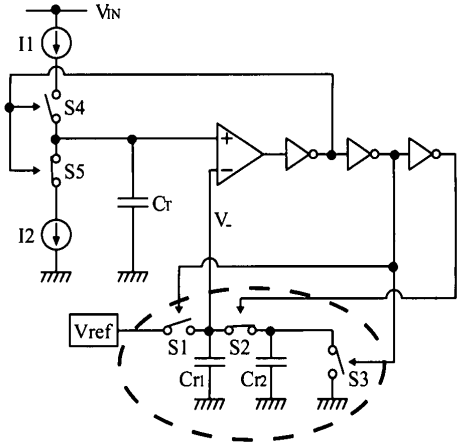

Fig. 23 1 MHz triangular waveform generator.

where β_1 is the transconductance parameter and V_{thd} is the threshold voltage of M1. V_{thd} has a negative value. I_1 is mirrored to I_2, which flows in M2. I_2 is expressed as,

$$I_2 = \frac{\beta_2}{2}(V_{gsM2} - V_{thM2})^2 \tag{19}$$

If $I_1 = I_2$ is chosen, then,

$$V_{gsM2} = V_{thM2} - \sqrt{\frac{\beta_1}{\beta_2}}V_{thd} \tag{20}$$

is obtained. Further assume that $\beta_1 = \beta_2$, then

$$V_{gsM2} = V_{thM2} - V_{thd} \tag{21}$$

Threshold voltages V_{thM2} and V_{thd} have different values, of course, but have the same temperature dependence to the 1st order approximation. Therefore, V_{gsM2} becomes temperature-independent and becomes less than 1 V. Although the V_{th} values change, the V_{ref} can be set to 1.0 V by adjusting the resistor values R_1 and R_2 that utilize the fuse ROMs.

Figure 23 shows the 1 MHz triangular oscillator that supplies the fixed time interval to the system. This is the relaxation-type oscillator. Two capacitors and three analog switches are used to generate two fixed-voltage values for realizing a hysteresis comparator.

When S_1 and S_3 turn on while S_2 is open, C_{r1} is charged to V_{ref} and C_{r2} is discharged to the ground. Then V_- becomes V_{ref}. When S_2 is turned on while S_1 and S_3 are turned off, the charge stored in C_{r1} is re-distributed to C_{r1} and C_{r2}. If $C_{r1} = C_{r2}$, then V_- becomes $V_{ref}/2$. As V_{ref} is a supply- and temperature-independent voltage, these two fixed voltages are stable. Therefore, the circuit can produce a stable 1 MHz triangular waveform.

The designed circuit has a feature to prevent the reverse current flow. Figure 24 summarizes the performance of the developed 1 MHz DC-DC converter with a 1 V output for 3.6 V and 2.5 V input voltages. The IC was fabricated by 2 μm CMOS technology. After

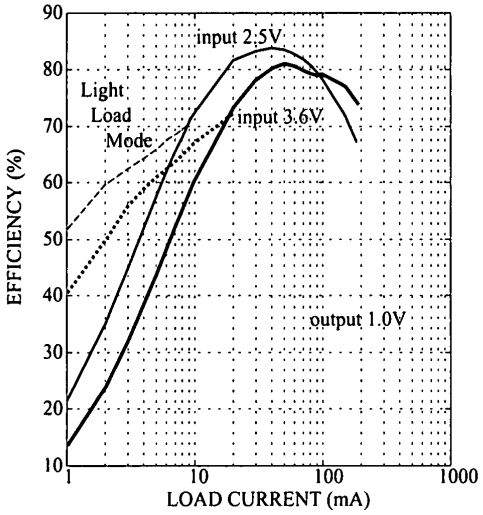

Fig. 24 Power efficiency.

stepping down from 3.6 V to 1.0 V, a power efficiency of more than 80% at load currents from 30 to 60 mA is observed. When the output power is 30 mW, the power consumed in a converter IC is 7.5 mW. At the point where the reverse current occurs in the light load mode, the protection circuit is activated and the efficiency is improved, as shown in Fig. 24. In this way, a power-efficient converter adequate for supplying energy to 1 V operational LSIs has been realized.

7. Conclusion

The supply voltage and the power dissipation of logic LSIs are decreasing rapidly. However, analog LSIs have not been able to keep up with these trends, because of the difficulty of implementing low-voltage and low-power operation. This paper demonstrates the possibility of reducing the supply voltage of analog LSIs while preserving their performance characteristics at almost the same level as before. Drastic power reduction is still the dream. The development of many low-voltage and low-power analog circuits for various applications is now needed.

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