A 1.5-V Current-Mode CMOS Sample-and-Hold IC with 57-dB S/N at 20 MS/s and 54-dB S/N at 30 MS/s

Yasuhiro Sugimoto, *Member, IEEE*

***Abstract*—A new video-speed current-mode CMOS sample-and-hold IC has been developed. It operates with a supply voltage as low as 1.5 V, a signal-to-noise ratio (S/N) of 57 dB and 54 dB with a 1-MHz input signal at clock frequencies of 20 and 30 MHz, and a power dissipation of 2.3 mW. It consists of current-mirror circuits with the node voltages at the input and the output terminals which are kept constant in all phases of the input signal by the use of low-voltage operational amplifiers; this reduces the signal current dependency. The low-voltage operational amplifier consists of a MOS transistor and a constant current source in a common-gate amplifier configuration. Only two analog switches in differential form were used to construct the differential sample-and-hold circuit. This minimizes the error caused by the switch feedthrough, and thus high accuracy can be realized. Since there is no analog switch in the input path, it is possible to convert the input signal voltage to a current by simply connecting an external resistor. The circuit was fabricated using standard 0.6-μm MOS devices with normal threshold voltages ($V_{\rm th}$) of +0.7 V (nMOS) and −0.7 V (pMOS).**

***Index Terms*—CMOS, current-mode circuit, low voltage, sample-and-hold.**

I. Introduction

LARGE-SCALE integrated (LSI) supply voltages are presently decreasing because LSIs are severely limited by device breakdown voltages and because they must achieve low power dissipation. However, it is usually difficult to lower the voltage of analog circuits while preserving high-precision and high-speed characteristics. The signal-to-noise ratio (S/N) and distortion deteriorate when the voltage range available for the signal is reduced. Our approach to solving this problem uses the signal current instead of signal voltage as the information carrier [1]. Although S/N is limited to a certain extent in current-based circuits [2], low-power and low-voltage operation is possible because the voltage change in each node is suppressed. Furthermore, high-speed operation is possible because the impedance of each node decreases. The high-speed operational capabilities of a current-based analog circuit have been previously demonstrated [3], [4]. The study referred to in [3] realized an 8-bit 15-MHz analog-to-digital (A/D) converter with a 5-V supply voltage by adopting the differential configuration of a switched-current circuit. The study referred to in [4] realized 57 MHz and 10-bit differential accuracy for a sample-and-hold circuit with a 3.3-V supply voltage by using the fixed-node voltages concept and the differential configuration of a BiCMOS switched-current circuit. However, supply voltages of those circuits were still high when we consider their integration with low-voltage digital circuits on the same chip. The noise level that appeared in the spectral plot in the former study was −66 dB with a read bandwidth of 300 Hz and that in the latter study was −67 dB with a read bandwidth of 290 Hz. These values are probably not sufficient for processing a wide-band input signal such as a picture signal. Moreover, the output of an operational amplifier in the latter study, which fixes the node voltage, begins floating in the hold mode of the current. This probably degrades the noise performance. These factors indicate that it is still difficult to realize a low-voltage accurate analog circuit together with high-speed operational capability.

In this paper, we propose the use of a conventional current-mirror-based circuit and minimum use of an analog switch to realize a high-speed and accurate low-voltage sample-and-hold circuit intended to be used for picture signal processing. The input and output voltages of the current-mirror circuit are kept constant to obtain accurate current matching. A new low-voltage operational amplifier was used to fix the node voltages of the current-mirror circuit. Only two analog switches are used in the differential configuration of this current-mirror based circuit. The input voltage-to-current conversion is thus simplified by connecting an external resistor between the signal and the input terminal. In order to demonstrate this, we designed and evaluated an MOS sample-and-hold IC that realizes 1.5-V operation, 20-MHz sampling with 57 dB of S/N, and 30-MHz sampling with 54 dB of S/N, and a power dissipation of 2.3 mW. The method used to obtain good current matching in the current-mirror circuit is described in Section II. The realization of a sample-and-hold circuit by using a low-voltage operational amplifier in a current-mirror-based circuit is discussed in Section III. Section IV introduces the entire designed circuit, which was fabricated using the 0.6-μm MOS process. Section V reports the evaluation results, and Section VI concludes our research.

II. Accurate Current-Mirror Operation

The current-mirror circuit is the basic circuit component in this current-based sample-and-hold IC. First, we analyzed the current transfer characteristic of the current-mirror circuit when the input signal current was applied. Fig. 1(a) shows the conventional MOS current-mirror circuit, which can operate with a very low supply voltage. M1 and M2 form a simple current-mirror circuit. Input signal current $i_{\rm in}$ and a constant bias current J are applied to the IN terminal, and a load resistor Rout is connected to the output terminal OUT. This current mirror generates

Manuscript received June 21, 2000; revised November 28, 2000.

The author is with the Department of Electrical, Electronic, and Communication Engineering, CHUO University, Tokyo 112-8551, Japan.

Publisher Item Identifier S 0018-9200(01)02400-3.

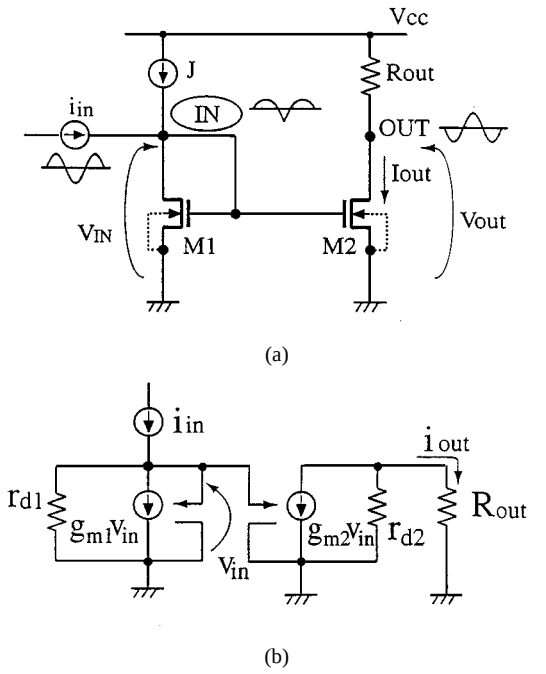

Fig. 1. (a) Conventional current-mirror circuit. (b) Small-signal equivalent circuit for input signal dependency analysis.

a large signal-dependent current conversion error. The voltages at terminals IN ($V_{\rm IN}$) and OUT ($V_{\rm OUT}$) become

$$V_{\rm IN} = \sqrt{\frac{2(J+i_{\rm in})}{\beta}} + V_{\rm th} \tag{1}$$

$$V_{\rm OUT} = V_{CC} - (J+i_{\rm in})R_{\rm OUT} \tag{2}$$

assuming $I_{\rm OUT}$ is equal to $J+i_{\rm in}$. Here β is a transconductance parameter, and $V_{\rm th}$ is the threshold voltage of the transistor.

Equations (1) and (2) indicate that the voltages at the IN and OUT terminals change depending on the input signal current $i_{\rm in}$, as shown in the figure. The voltage at terminal IN changes nonlinearly. Moreover, the directions in which these voltages change are opposite, and the drain-to-source voltage $V_{\rm DS}$ of M1 and M2 do not become equal in any phase of the input signal. Since the transconductance g_m and the output resistance r_d of the transistor are expressed as

$$g_m = \sqrt{2\beta I_d(1+\lambda V_{\rm DS})} \tag{3}$$

$$r_d = \frac{(1+\lambda V_{\rm DS})}{\lambda I_d} \tag{4}$$

where I_d is the drain-to-source current and λ is the channel modulation factor of the transistor, the g_m's and r_d's of M1 and M2 do not become equal and thus introduce a current transfer error.

Assuming the voltage changes are small, this situation can be analyzed by using a small-signal equivalent circuit, as shown in Fig. 1(b). Here, the output current $i_{\rm out}$ becomes

$$i_{\rm out} = -\left[\frac{g_{m2}}{g_{m1}+(1/r_{d1})}\right]\left[\frac{1}{1+(R_{\rm out}/r_{d2})}\right] i_{\rm in} \tag{5}$$

where g_{mx} (x is 1 or 2) is the transconductance and r_{dx} (x is 1 or 2) is the output resistance of M1 and M2. Equation (5) indicates that $i_{\rm out}$ does not become equal to $i_{\rm in}$ even when $g_{m1} \gg (1/r_{d1})$ and $1 \gg (R_{\rm out}/r_{d2})$, due to the different g_m's

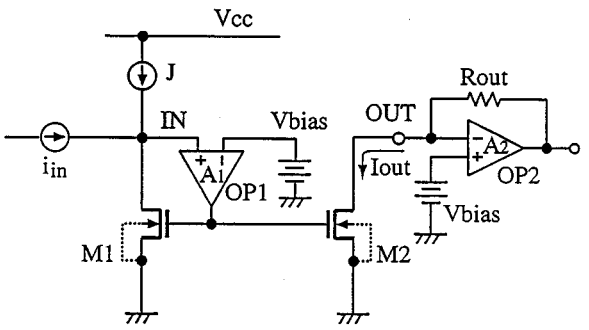

Fig. 2. High-precision current-mirror circuit.

of M1 and M2. The situation worsens when the influence of $1/r_{d1}$ and $R_{\rm out}/r_{d2}$ cannot be ignored. Therefore, the circuit in Fig. 1(a) fundamentally produces a current transfer error.

In order to solve this problem, we used the concept of keeping the input and the output terminal voltages of a current-mirror circuit constant by adding two operational amplifiers, as shown in Fig. 2. The concept of using an amplifier to maintain constant equal $V_{\rm DS}$ across both sides of a current mirror circuit is as old as the concepts in Fig. 3 of the study referred to in [4] and in the study referred to in [5, Fig. 14.2]. Our circuit in Fig. 2 is in a form in which two operational amplifiers are simply added to the conventional current-mirror circuit. We adopted this configuration because only one analog switch is necessary to realize a sample-and-hold function. We will discuss this issue later. In Fig. 2 of this paper, operational amplifier 1 (OP1) is inserted between the IN terminal and the gates of transistors M1 and M2, and operational amplifier 2 (OP2) is connected in parallel to the resistor Rout. The bias voltages for OP1 and OP2 are the same and are $V_{\rm bias}$. The terminal voltages of IN and OUT terminals then become equal to $V_{\rm bias}$ due to the feedback operation of OP1 and OP2. The g_m's and r_d's of M1 and M2 become equal, though their values change as the input current changes. The effects of inserting these operational amplifiers are that g_{m1} becomes $A_1 g_m$, g_{m2} becomes $A_1 g_m$, and $R_{\rm out}$ becomes $R_{\rm out}/A_2$ in (5). G_{m1} and g_{m2} become equal to g_m, and r_{d1} and r_{d2} to r_d, because all the terminal voltages of M1 and M2 are now equal. Thus, (5) becomes

$$i_{\rm out} = -\left[\frac{g_m}{g_m+(1/A_1 r_d)}\right]\left[\frac{1}{1+(R_{\rm out}/A_2 r_d)}\right] i_{\rm in}. \tag{6}$$

When A_1 and A_2 are sufficiently large, $i_{\rm out}$ in (6) becomes exactly equal to $i_{\rm in}$. $I_{\rm out}$ is not affected by the change of the g_m and the r_d accompanied with a signal current change. The problem to be considered next is how to design an operational amplifier and a sample-and-hold switch under very low voltage supply conditions.

III. Realization of a Low-Voltage High-Performance Sample-and-Hold Circuit

The designed sample-and-hold circuit is conceptually depicted in Fig. 4. The input signal is assumed to be in voltage form in this configuration; therefore, an input voltage-to-current conversion circuit is required. This can be achieved by simply connecting an external resistor $R_{\rm in}$ between the input

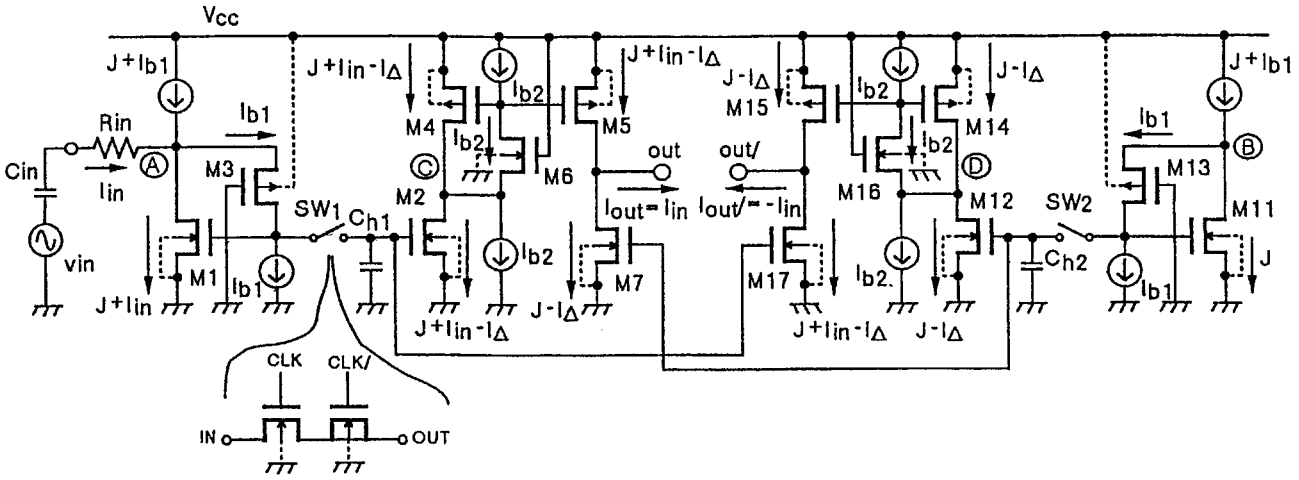

Fig. 3. Current-mode low-voltage high-performance CMOS sample-and-hold circuit.

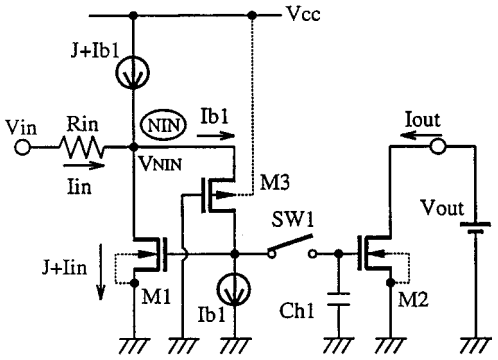

Fig. 4. High-precision low-voltage sample-and-hold circuit.

signal and the terminal NIN in the figure, because the voltage at terminal NIN does not change in any phase of the input signal. A precise voltage-to-current conversion is achieved in this way. A sample-and-hold operation is performed by using analog switch SW1 and hold capacitor Ch1. In sample mode, SW1 is turned on, and the gates of transistors M1 and M2 become connected. Precise current-mirroring operation occurs if the drain voltages of both transistors are the same. Therefore, $i_{\rm out}$ becomes a replica of $i_{\rm in}$. Ch1 memorizes the gate voltage of M2 just before SW1 turns off. PMOS transistor M3, with its bulk terminal connected to V_{cc} and gate terminal to ground, together with current source Ib1, forms a positive amplifier, or OP1 in Fig. 2.

The current-based sample-and-hold circuit has been previously reported in [4, Fig. 4] and [5, Fig. 14.2]. Their circuits use three analog switches, operational amplifiers to fix node voltages, and only one transistor for storing and playing back current. The use of one transistor is preferable because it becomes free of the transistor's parameter variation. However, the use of three analog switches is not preferable from the switch feedthrough error point of view. Moreover, the output of the operational amplifier in [4, Fig. 4] begins to float in hold mode. It may affect the voltage held by the hold capacitor. This floating condition eventually occurs also in the circuit in [5, Fig. 14.2] when only one current source is used. As this circuit is configured as a parallel current sample/hold/summer, the time for the operational amplifier to begin floating and for the output terminal of the current source to deviate is short. However, they still float and deviate when switches change from one current source to another because switches are commonly controlled by nonoverlapping clocks. Our conclusion from these previous works is that we need to avoid those floating or deviating conditions at all times. It is also necessary for our circuit to operate at a very low voltage. The circuit in Fig. 4 in this paper satisfies those requirements, though it may be affected by the device parameter mismatch.

In Fig. 4, current $(J + I_{\rm in})$ flows in n-channel transistor M1, while $V_{\rm NIN}$ at terminal NIN is fixed by the gate-to-source voltage of p-channel transistor M3. The current through transistor M3 is a constant current I_{b1}; therefore, its gate-to-source voltage remains constant. In this configuration, the A_1 in (6) becomes

$$A_1 = \frac{g_{m3}}{g_{\rm ds3}} \tag{7}$$

where g_{ms3} and $g_{\rm ds3}$ are the transconductance and the output conductance, respectively, of transistor M3. The voltage at the drain terminal of M2 ($V_{\rm out}$) is assumed to be kept constant because it is the output terminal of the sample-and-hold circuit. An external operational amplifier and an external resistor are connected in parallel for actual evaluation, as shown in Fig. 2. The voltage $V_{\rm out}$ is adjusted to become equal to that of $V_{\rm NIN}$. However, M3 may possibly enter the linear region in this configuration. Care must be taken to avoid this situation because g_{m3} decreases while $g_{\rm ds3}$ increases, and thus A_1 is greatly reduced in (7). The voltage $V_{\rm NIN}$ at terminal NIN and the drain-to-source voltage $V_{\rm ds3}$ of M3 are calculated as

$$V_{\rm NIN} = |V_{\rm thp}| + \sqrt{\frac{2I_{b1}}{\beta_p}} \tag{8}$$

$$V_{\rm ds3} = V_{\rm NIN} - V_{\rm thn} - \sqrt{\frac{2J}{\beta_n}} \tag{9}$$

provided that $J > I_{\rm in}$. $V_{\rm thp}$ and β_p are the threshold voltage and the transconductance parameter of M3, respectively, and $V_{\rm thn}$

and β_n are those for M1, respectively. The following conditions are required for M3 to operate in the saturation region.

$$|V_{\rm thp}| > V_{\rm thn} + \sqrt{\frac{2J}{\beta_n}}. \tag{10}$$

M3's bulk terminal is connected to V_{cc} in this design, and M3's source terminal is connected to terminal NIN. This gives rise to the bulk effect, and $V_{\rm thp}$ becomes large. Therefore, the condition required in (10) is satisfied.

The minimum supply voltage of the circuit in Fig. 4 becomes $V_{\rm NIN}$ plus the voltage necessary to maintain a current source $J+I_{b1}$. With a $V_{\rm thp}$ of -1 V, considering the bulk effect of M3, the minimum supply voltage is estimated to be roughly 1.5 V.

IV. Designed Differential Sample-and-Hold Circuit

We designed the current-mode CMOS sample-and-hold circuit shown in Fig. 3. An input signal current of ± 200 μA (full scale) is applied to terminal A through an external resistor $R_{\rm in}$. The circuit in Fig. 4 suffers greatly from clock feedthrough error from an analog switch. Differential placement of sample switches and cancellation of the clock feedthrough are necessary [6]. The drain voltages of transistors M2 and M12 are kept constant by using the replica pMOS version of the circuit in Fig. 4 to achieve signal-independent current-mirror operation. Now, voltages at terminals A, B, C, and D in Fig. 3 are constant. Voltages at the out and out/ terminals are also kept constant because these terminals are assumed to be connected to the virtual ground of external operational amplifiers in the evaluation and to the same kind of constant voltage input terminals when this sample-and-hold circuit is used in combination with a current-mode A/D converter. Therefore, the currents flowing in M2, M4 and M5 are set to be equal. The voltage across Ch1 changes when a clock feedthrough error is generated in SW1. Suppose that a current change $-\Delta I$ occurs in M2 due to the voltage change at Ch1. The currents flowing through M17, M4, and M5 then also change by $-\Delta I$. Since the same amount of clock feedthrough is expected to be injected from SW2 to Ch2, the same degree of current change as in M2 ($-\Delta I$) is considered to be generated in M12, M7, M14, and M15. The current change caused by the switches' clock feedthrough in M5 is $-\Delta I$, and that in M7 is also $-\Delta I$. These two current changes cancel each other, and the clock feedthrough will not influence the output current $I_{\rm out}$. The same kind of clock feedthrough cancellation occurs at terminal out/.

Even when there are parameter mismatches among transistors, this cancellation is still effective. Clock feedthrough injected to Ch1 in Fig. 3 is amplified and converted into a current by M2. The error current is mirrored by M4 and M5 and appears at the terminal out. The current transfer ratio error of a current mirror is at most a few percents. The error current caused by the clock feedthrough injection to Ch2 also appears at the terminal out. As the differences between these two are taken at the out terminal, the resultant error current decreases compared with the original one. The same discussion holds for the error current at the out/ terminal.

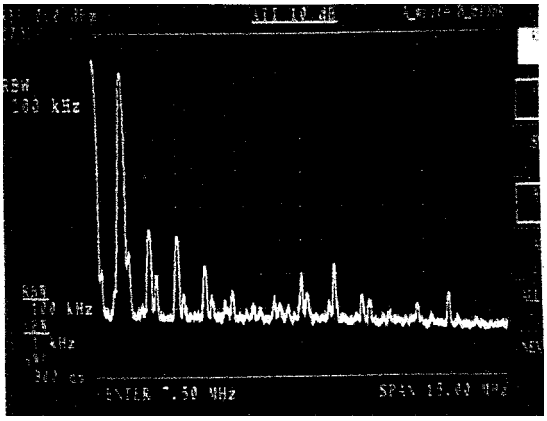

Fig. 5. Spectrum of the output signal (differential) (fin = 1 MHz, 0 dB full scale input, V_{cc} = 1.5 V, clock = 30 MHz, RBW = 100 KHz, VBW = 1 KHz, span = 15 MHz).

The supply voltage of the circuit in Fig. 3 is still as low as 1.5 V. When the circuit is operated with that voltage, node voltages between terminal A and terminal C, for example, do not become equal. The voltage at terminal C becomes a few hundred millivolts while that at terminal A becomes about 1.2 V; therefore, the current mirror ratio between M1 and M2 is smaller than one. On the other hand, almost the same amount of current transfer error occurs between M11 and M12. As a result, the same amount of offset current error appears at both terminals out and out/. As out and out/ terminals are assumed to be connected to the external operational amplifiers, and the signals are further amplified in a differential manner, those offset currents can be canceled. However, the output signals may contain harmonics in this case because the current mirror ratio is not one. If the same node voltages at terminals A and C, or B and D, in Fig. 3 are required, then the circuit needs the 2.5-V supply voltage.

From the stability point of view, the circuits used in Fig. 3 with 100% of negative feedback always have a possibility of oscillation. Care must be taken in designing the loop gain so that it does not have the peak in frequency characteristic. The input circuit which consists of transistors M1 and M3 and current sources $J+I_{b1}$ and I_{b1} has less possibility of oscillation because the voltage gain of M1 decreases when the resister $R_{\rm in}$ is connected to the terminal A. Other circuits in Fig. 3, however, still have this possibility. We sometimes need to include capacitors to prevent oscillation.

V. Experimental Results [7]

The circuit in Fig. 3 was fabricated using CMOS 0.6-μm devices. NMOS transistors have a $V_{\rm th}$ of $+0.7$ V, and pMOS transistors, -0.7 V. Fig. 5 illustrates the frequency spectrum of the output waveform with a 30-MHz clock with a supply voltage of 1.5 V. The input signal was full scale with a frequency of 1 MHz. The RBW was 100 kHz; the VBW, 1 kHz; and the frequency span, 15 MHz. The observed noise level was -85 dBm, while the fundamental, second, and third harmonics were -10, -58, and -59 dBm, respectively. The S/N was calculated as 54 dB, while the second and third harmonic became -48 and -49 dB, respectively, as referred to the output signal

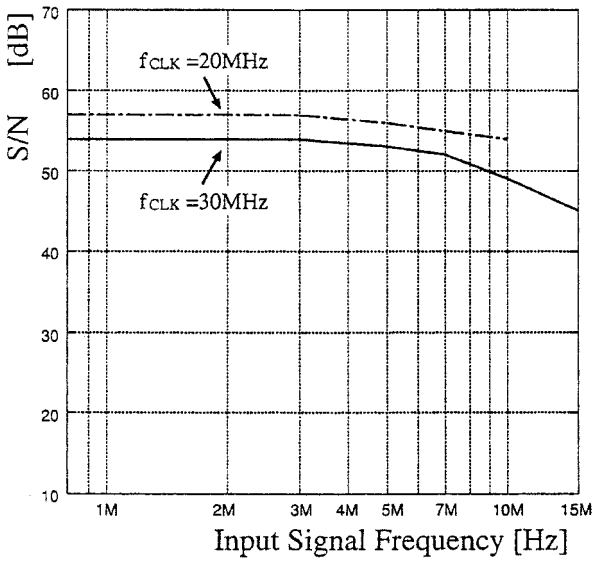

Fig. 6. Input signal frequency versus S/N characteristics (0-dB full-scale input, $V_{cc} = 1.5$ V).

level. These second and third harmonic levels are not small enough when this sample-and-hold circuit is used in front of a 9- or 10-bit current-mode A/D converter. We are not concerned about any input signal dependency on the on resistance of the analog switches in this sample-and-hold circuit, which may influence the harmonics level. The supply voltage for the logic gates, which drives the gates of the analog switches, can be set to over 1.5 V in this chip, within the range where the parasitic diode does not conduct. Since we observed a 5-dB improvement in the second and third harmonic levels when the gate voltage of the analog switches was raised to 1.8 V, the on resistance of the analog switches is not small enough with a 1.5 V of supply voltage. The circuit simulation also indicates that the harmonics level greatly depends on the I_{b1} value in Fig. 3. We chose an Ib1 value of 25 μA. We may need to boost the gate voltages of the analog switches and increase the I_{b1} value to obtain a satisfactory result in the future.

Fig. 6 shows the S/N with a changing input signal frequency in the sample-and-hold mode. The bold line shows the S/N value when the clock frequency is 30 MHz; the dotted line shows the S/N with a 20-MHz clock. The S/N at a low frequency reached 54 and 57 dB for clocks at 30 and 20 MHz, respectively. Even a 15-MHz input signal did not significantly degrade the S/N. We can conclude that the S/N was a 9-bit level for a 30-MHz clock and a 10-bit level for a 20-MHz clock.

TABLE I
OVERALL CHIP PERFORMANCE

Item	Value	Unit
Vcc	1.5	V
S/N 1MHz , clock 30MHz	54	dB
15MHz , clock 30MHz	45	dB
1MHz , clock 20MHz	57	dB
Distortion 1MHz input 2nd clock 30MHz	-48	dB
Power dissipation	2.3	mW
Process	CMOS 0.6μm	
Vth NMOS	+0.7	V
PMOS	-0.7	V

Table I summarizes the chip's overall performance. The power dissipation was 2.3 mW.

VI. CONCLUSION

We were able to demonstrate 1.5-V operation of a 30-MS/s CMOS current-mode sample-and-hold circuit. This was achieved using transistors with normal $V_{\rm th}$ values. We are confident that a 1.5-V operational and accurate analog circuit for video use can now be realized by applying this current-based circuit technique.

REFERENCES

[1] C. Toumazou, J. B. Hughes, and N. C. Battersby, *Switched Currents: an Analogue Technique for Digital Technology*. Stevenage, U.K.: Peregrinus, 1993.
[2] Y. Sugimoto, M. Sekiya, and T. Iida, "A study of the signal-to-noise ratio of a high-speed current-mode CMOS sample-and-hold circuit," *IEICE Trans. Fundamentals*, vol. E80-A, no. 10, pp. 1986–1993, Oct. 1997.
[3] M. Bracey, W. Redman-White, J. Richardson, and B. Hughes, "A full Nyquist 15-MS/s 8-b differential switched-current A/D converter," *IEEE J. Solid-State Circuits*, vol. 31, pp. 945–951, July 1996.
[4] X. Hu and K. W. Martin, "A switched-current sample-and-hold circuit," *IEEE J. Solid State Circuits*, vol. 32, pp. 898–904, June 1997.
[5] C. Toumazou, F. J. Lidgey, and D. G. Haigh, Eds., *Analogue IC Design: The Current-Mode Approach*. Stevenage, U.K.: Peregrinus, 1990.
[6] Y. Sugimoto, S. Tokito, H. Kakitani, and E. Seta, "A current-mode bit-block circuit applicable to low-voltage low-power pipeline video-speed A/D converters," *IEICE Trans. Fundamentals*, vol. E79-A, no. 2, pp. 199–209, Feb. 1996.
[7] Y. Sugimoto, "A 1.5-V 30-Msps 9- to 10-bit equivalent current-mode CMOS sample-and-hold circuit," in *Proc. 25th Eur. Solid-State Circuits Conf.*, Sept. 1999, pp. 378–381.