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Design of a Sub-1.5 V, 20 MHz, 0.1% MOS Current-Mode Sample-and-Hold Circuit

YASUHIRO SUGIMOTO, *Member* **AND MASAHIRO SEKIYA,** *Nonmember*

The Department of Electrical and Electronics Engineering, Chuo University, Tokyo, 112-8551 Japan

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Abstract. This paper describes an MOS current-mode sample-and-hold (S/H) circuit that potentially operates with a sub-1.5 V supply voltage, 20 MHz clock frequency, and less than 0.1% linearity. A newly developed voltage-to-current converter suppresses the voltage change at an input terminal and achieves low-voltage operation with superior linearity. Sample switches are differentially placed at the inputs of a differential amplifier so that the feed through errors from switches cancel out. The MOS current mode S/H circuit is designed and simulated using CMOS 0.6 μm device parameters. Simulation results indicate that an operation with 20 MHz clock frequency, linearity error of less than 0.1%, and 1 MHz input from a 1.5 V power supply is achievable.

Key Words: low voltage, high speed, high accuracy, MOS analog circuit, sample-and-hold circuit

1. Introduction

In the coming digitally-oriented era, analog circuits will continue to be used for interfacing with the real analog world, for high-frequency applications, and even in high-speed digital LSIs. Although digital LSIs can operate with reduced supply voltage and achieve low power dissipation even in smaller devices, analog LSIs cannot. And although the reduction of supply voltage is a crucial constraint of analog circuits (which process information in voltage form), this reduction can be expected to continue [1]. In the coming era, therefore, it will be necessary to realize high-performance analog functions, such as a video-rate A/D converter, under condition of a supply voltage as low as 1 V. In this paper, we investigated the possibility of realizing such an analog function by adopting a current-mode circuit approach in which information is processed in current form. A new sample-and-hold circuit that can operate with sub-1.5 V supply voltage, 20 MHz clock frequency, and more than 10-bit level accuracy has been designed and simulated using CMOS 0.6 μm device parameters.

2. A New High-Performance Input Voltage-to-Current Converter

Even when the supply voltage is reduced, the levels of performance of analog circuits must be maintained. In a conventional current-mode circuit, the input voltage-to-current conversion is achieved by use of an operational amplifier (op-amp) with very high gain at a high frequency. This is not possible under conditions of a low supply voltage, because there is not enough voltage for an op-amp to maintain high gain at a high frequency. Therefore, a low-voltage and high-performance input voltage-to-current converter is needed. Fig. 1(a) shows the conventional circuit as one candidate for this purpose [2]. In this configuration, the input current I_{in} and a constant current J together flow in the transistor M1, which produces a small voltage change at a terminal IN when I_{in} changes. The voltage change is then used to reproduce a current change, which is exactly the same as I_{in}, at another terminal. The voltage V_{IN} at the terminal IN becomes

$$V_{IN} = V_{thn} + \sqrt{2J/\beta_n} \tag{1}$$

where V_{thn} is the threshold voltage of an n-channel transistor M1 and β_n is its transconductance parameter. The minimum supply voltage approaches 1 V

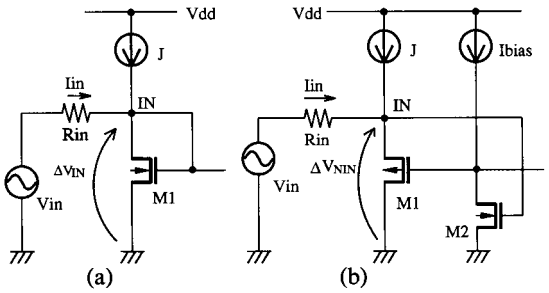

Fig. 1. Input voltage-to-current converters (a) Conventional circuit. (b) Newly developed circuit.

in this circuit. On the other hand, the voltage change ΔV_{IN} at the terminal IN is

$$\Delta V_{IN} = I_{in}/g_{m1} \cong I_{in}/\sqrt{2\beta_n J} \tag{2}$$

where g_{m1} is the transconductance of the transistor M1. This means that the equivalent input current is reduced due to the voltage change. In addition to this, the voltage change is not precisely proportional to the input current change, and it introduces distortion. What is needed is an input voltage-to-current converter the input terminal voltage of which is not dependent on I_{in}. Fig. 1(b) shows a new circuit for avoiding this problem. Here, I_{in} and J flow in a p-channel transistor M1, while V_{IN} at a terminal IN is set by the gate-to-source voltage of n-channel transistor M2. The current through transistor M2 is now the constant current I_{bias} and, therefore, its gate-to-source voltage remains constant. The input voltage change ΔV_{NIN} becomes

$$\Delta V_{NIN} = (g_{ds2}/g_{m1}g_{m2})I_{in} \tag{3}$$

where g_{m2} and g_{ds2} are transconductance and output conductance of a transistor M2. Equation (3) indicates that ΔV_{NIN} is much smaller than ΔV_{IN} in equation (2) by the amount of g_{ds2}/g_{m2}. In this way, the voltage change appearing at the terminal IN is suppressed. Now the voltage change appears at the gate of M1, and the input current change can be re-produced by using this voltage change. The voltage V_{1Nnew} at a terminal IN and drain-to-source voltage V_{dsM2} of M2 becomes

$$V_{INnew} = V_{thn} + \sqrt{2I_{bias}/\beta_n}$$

$$V_{dsM2} = V_{INnew} - |V_{thp}| - \sqrt{2J/\beta_p} \tag{4}$$

where V_{thp} and β_p are the threshold voltage and the transconductance parameter of M2. In order to enable M2 to operate in the saturation region, the condition

$$V_{dsM2} > \sqrt{2I_{bias}/\beta_n}$$

that is,

$$V_{thn} > |V_{thp}| + \sqrt{2J/\beta_p}$$

is required. In this design, a transistor with low V_{th} value is available at the same time as a transistor with normal V_{th} value. The device parameters used for this simulation were obtained from the measurement data of actual 0.6 μm MOS devices. V_{thn} becomes 0.9 V and V_{thp} becomes -0.2 V. Because $\sqrt{2I_{bias}/\beta_n}$ becomes about 0.2 V, V_{INnew} is calculated as 1.1 V. This implies that the circuit could be operated with a supply voltage of less than 1.5 V, assuming that 0.4 V is needed to form the current source J. Fig. 2 shows the results of a SPICE simulation in which ΔV_{IN} in equation (2) and ΔV_{NIN} in equation (3) are compared. Current values of sources J and I_{bias} are set at 100 μA and 40 μA, respectively, and I_{in} changes from $\pm$ 10 μA to $\pm$ 90 μA. A voltage suppression ratio of greater than 50 is obtained.

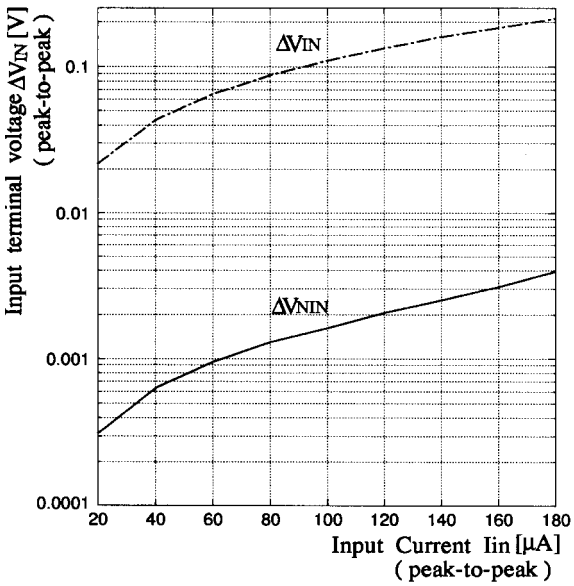

Fig. 2. Voltage change at input terminals in circuits of Fig 1(a) and (b) with various input currents.

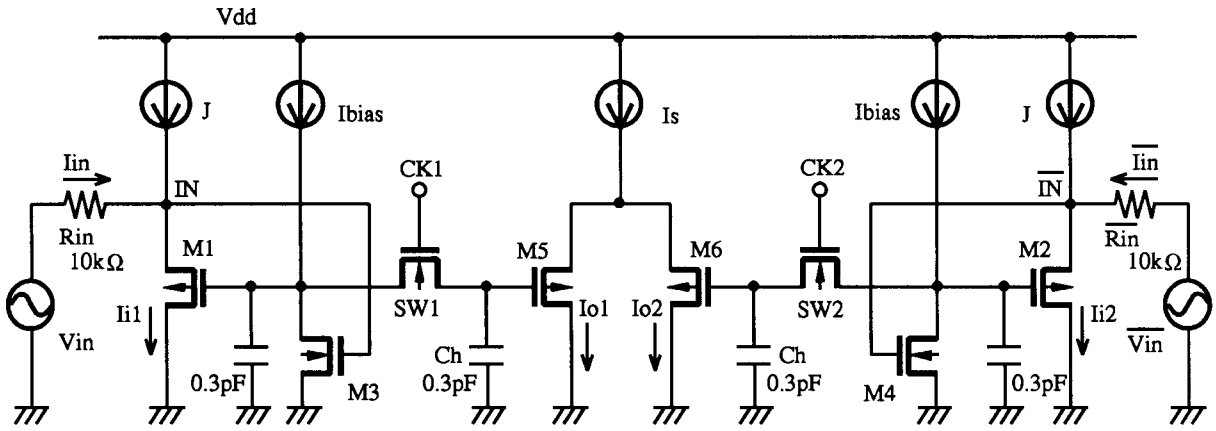

Fig. 3. Designed sample-and-hold circuit.

3. A Current-Mode Sample-and-Hold Circuit

The low-voltage, high-performance and high-speed sample-and-hold circuit shown in Fig. 3 was designed by utilizing the circuit in Fig. 1(b). Two input voltage-to-current converters are placed in differential form. When I_{in} and $I_{in}/$ are applied to the IN and IN/ terminals, respectively, the correspondent difference voltage change appears between the gates of M1 and M2. This voltage change is converted back to the output currents by the differential amplifier, M5 and M6. Since the voltage change at IN and IN/ terminals is greatly reduced, the gate-to-source voltages of M5 and M6 become exactly the same as those of M1 and M2 when I_s is selected as *2J*. Therefore, the output currents I_{o1} and I_{o2} become equal to I_{in} and $I_{in}/$, respectively. The difference current $I_{o1} - I_{o2}$ is then used to obtain an output current which is free of clock feedthrough error. Although the circuit for this output current generation is not shown in the figure, it can be realized by using a folded-cascode type output circuit, as is illustrated in [3]. This is because roughly 0.5 V of the gate-to-drain voltage difference remains in M5 or M6. SW1, SW2, and the two C_h capacitors form sample switches that enable the sample-and-hold operation. When the switches are turned off, the voltages are kept in the C_h capacitors, and I_{o1} and I_{o2} become constant. The differential placement of switches is very effective at suppressing the clock feedthrough error caused by sample switches [3]. The circuit in Fig. 3 was designed using CMOS 0.6 μm device parameters. It is an n-well CMOS process and all the bulk terminals of PMOS transistors are tied to the V_{dd} terminal. All the transistors except for M3 and M4 have a low V_{th} value of 0.2 V for NMOS and -0.2 V for PMOS. M3 and M4 have a threshold voltage of 0.9 V. In an actual circuit, the current sources in Fig. 3 are replaced by cascoded transistors. J, I_{bias}, $2I_s$ and C_h are 100 μA, 40 μA, 200 μA, and 0.3 pF, respectively, and R_{in} and $R_{in}/$ are 10 kΩ. Additional capacitors of 0.3 pF are connected between the gates of M1 and M2 to ground in order to avoid oscillation in the circuit. Total power dissipation of this circuit is calculated as 0.72 mW. The designed circuit is simulated with a 1.5 V supply voltage. Fig. 4

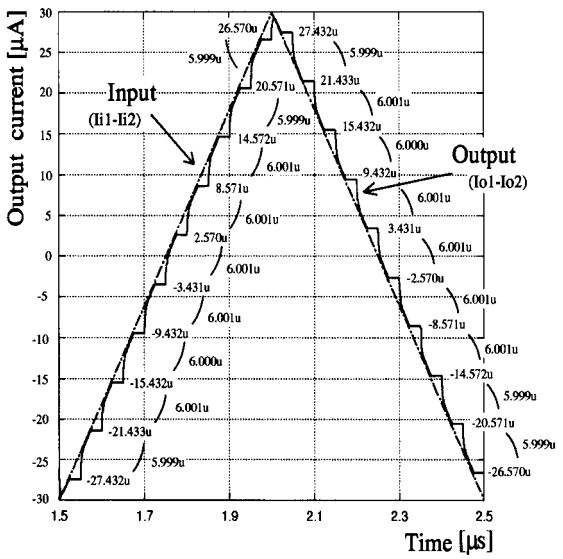

Fig. 4. Input- and output-current waveforms of the sample-and-hold circuit.

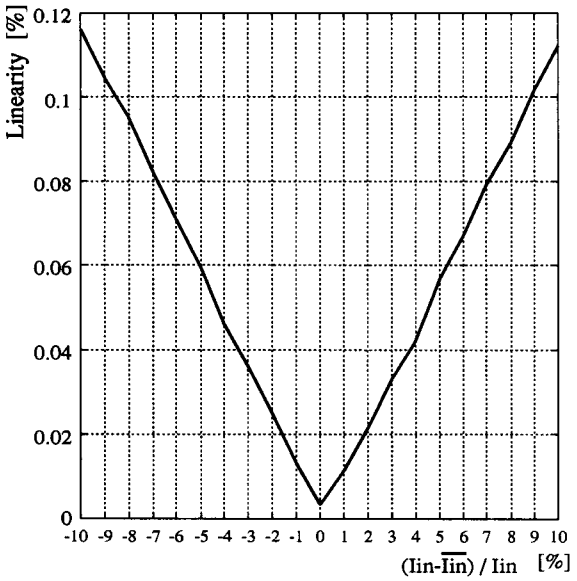

Fig. 5. Linearity degradation due to input signal unbalance.

shows input and output current waveforms with input frequency of 1 MHz and with a clock frequency of 20 MHz in sample-and-hold mode. The input current is equal to $I_{i1} - I_{i2}$ and the output current is equal to $I_{o1} - I_{o2}$ in Fig. 3. The I_{in} value is $\pm$ 15 μA in this case, resulting in a $\pm$ 30 μA change in both input and output current due to the differential operation. The desired difference current value between adjacent hold steps is 6.000 μA, and the simulated value ranges from 5.999 μA to 6.001 μA. This means the sample-and-hold circuit has a superior linearity of less than 0.1%. The proposed circuit is assumed to have the complementary input signals of I_{in} and $I_{in}/$. The connection point of sources of M5 and M6 becomes the virtual ground only when signals with equal magnitude in opposite polarity are applied to the inputs. Otherwise, the distortion and linearity degrade. The influence was simulated and is shown in Fig. 5. Linearity error is observed by changing the signal level of one of the inputs (I_{in} or $I_{in}/$) relative to the other. The results indicate that, even with 8 to 9% unbalance in the signal level, less than 0.1% of linearity can be obtained. Mismatches of the transistor threshold voltage also affect the circuit performance. In particular, the matching of transistors M1, M2, M5, and M6 is important. The influence of the V_{th} mismatch, already analyzed in [3], results in gain error, offset current production, and only a marginal degradation of linearity. Because the offset current becomes less important when the digital correction logic of an A/D converter is adopted, care must be taken to lower the gain error, as in layout design process. Throughout these investigations, a 10-bit level of sample-and-hold operation is found to be achievable at 20 MHz clock frequency with 1.5 V supply voltage.

4. Conclusion

A low-voltage and high-performance input voltage-to-current converter is presented and used to design a video-rate current-mode sample-and-hold circuit. The simulation of the circuit shows a 20 MHz operational capability with more than 10-bit level linearity from a 1.5 V supply voltage. This implies the possibility of high-performance and high-speed analog circuits operating at supply voltages of as low as 1 V.

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Yasuhiro Sugimoto (*Member*) received the B.E. degree from Tokyo Institute of Technology, Tokyo, Japan, M.E. degree from University of Michigan, Ann Arbor, Michigan, and Doctor of Engineering degree from Tokyo Institute of Technology, Tokyo, Japan, in 1973, 1980, and 1991, respectively. He joined Toshiba Semiconductor Group in 1973, and engaged in the

development of analog VLSIs. Since 1992, he has been with the Faculty of Science and Engineering, Chuo University where he is now a professor in the Department of Electrical and Electronic Engineering. His main interest is the design and development of new circuits in mixed analog and digital VLSIs. He is the recipient of the 1990 Best Paper Award of European Solid-State Circuits Conference. He is the author of two books. Dr. Sugimoto is a member of the Institute of Electrical and Electronics Engineers, INC., the Institute of Electrical Engineers of Japan and the Japan Consulting Engineers Association.