

# A Study of the Signal-to-Noise Ratio of a High-Speed Current-Mode CMOS Sample-and-Hold Circuit

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**SUMMARY** Our study investigated the realization of a high-precision MOS current-mode circuit. Simple studies have implied that it is difficult to achieve a high signal-to-noise ratio (S/N) in a current-mode circuit. Since the signal voltage at the internal node is suppressed, the circuit is sensitive to various noise sources. To investigate this, we designed and fabricated a current-mode sample-and-hold circuit with a 3 V power supply and a 20 MHz clock speed, using a standard CMOS 0.6  $\mu\text{m}$  device process. The measured S/N reached 57 dB and 59 dB in sample mode, and 51 dB and 54 dB in sample-and-hold mode, with  $\pm 115 \mu\text{A}$  from a 3 V power supply and  $\pm 220 \mu\text{A}$  from a 5 V power supply of input currents and a 10 MHz noise bandwidth. The S/N analysis based on an actual circuit was done taking device noise sources and the fold-over phenomena of noise in a sampled system into account. The calculation showed 66.9 dB of S/N in sample mode and 59.5 dB in sample-and-hold mode with  $\pm 115 \mu\text{A}$  of input current. Both the analysis and measurement indicated that 60 dB of S/N in sample mode with a 10 MHz noise bandwidth is an achievable value for this sample-and-hold circuit. It was clear that the current-mode approach limits the S/N performance because of the voltage suppression method. This point should be further studied and discussed.

**key words:** signal-to-noise ratio, noise analysis, sample-and-hold circuit, current-mode circuit, MOS analog circuit

## 1. Introduction

Low-voltage, low-power, high-frequency operation is required for today's LSI circuits. The mixed use of analog and digital circuits is also necessary; and a one-chip system requires the use of MOS transistors throughout the chip. It is usually difficult to make an MOS analog circuit operate with a reduced supply voltage, due to the dynamic range and gain reduction of the amplifier. Because conventional analog circuits process information in voltage form and there is not enough gate-to-source voltage for an MOS transistor, the analog performance degrades when the supply voltage is reduced. The use of current-mode (and/or switched-current) circuits has been extensively studied in order to overcome these limitations and achieve low-voltage, low-power, high-frequency operation [1]–[3]. Information is processed in current form in these circuits and impedance

at every node becomes low, thus enabling low-voltage and high-frequency operation. Therefore, the only practical choice for a future analog circuit design is the use of a current-mode circuit. However, Gilbert Cells often suffer from poor signal-to-noise ratios (S/N) [4]. Information is processed by utilizing a current mirror operation in a Gilbert Cell. In a current mirror circuit, the input current flows in the diode-connected transistor and the signal voltage is suppressed. This voltage is converted back and becomes the output current through the use of another transistor. The same kind of operation is found in a current-mode circuit, because it basically consists of many current mirrors. Since the voltage is suppressed and the signal is processed in current form, the S/N degrades when noise sources are added to the node which is the connection point between the diode-connected transistor and the gate of another transistor. Therefore, there must be a S/N limit. This point has not been previously investigated or clarified. To do this, we designed and fabricated a full current-mode sample-and-hold circuit by using 0.6  $\mu\text{m}$  CMOS process and measured its S/N characteristics. We conducted a noise analysis based on an actual designed circuit. The analysis and the measurement were consistent except for the S/N in sample mode. This paper discusses the substantial S/N limitation of a current-mode circuit. In Sect. 2, the S/N of a basic current-mirror circuit is analyzed. Section 3 describes the circuit of the designed full current-mode CMOS sample-and-hold test chip; Section 4 gives the measured results. Section 5 discusses the noise issue and the fundamental limitations of the current-mode approach, based on calculations and the measured S/N data. Section 6 concludes the paper.

## 2. Noise Analysis in a Basic Current Mirror Circuit

Since the current mirror circuit is the major functional component in a current-mode circuit, we first analyzed its S/N characteristic. Figure 1 shows a basic current mirror circuit with the transistors' noise sources. Input signal current  $I_{in}$  and constant current  $J$  flow together in diode-connected transistor M1. This current is copied exactly as the output current of M2, provided that the transistors are the same size. We considered only the voltage noise source at the input of the transistor, since the impedance at terminal IN is low [5]. In this configu-

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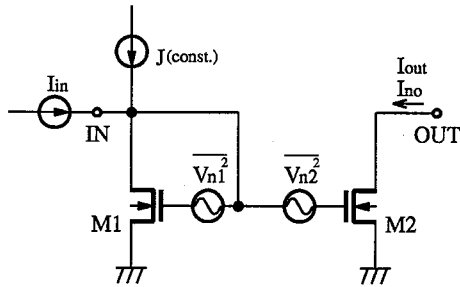


Fig. 1 A basic current mirror circuit with transistors' noise sources.

ration, the output noise current  $I_{no}$  and the transistor's noise  $V_n$  becomes

$$\begin{aligned} \overline{I_{no}^2} &= g_m^2 (\overline{V_{n1}^2} + \overline{V_{n2}^2}) = 2g_m^2 \overline{V_n^2} \\ \overline{V_n^2} &= (8kT/3g_m)\Delta f \end{aligned} \quad (1)$$

where  $k$  is the Boltzmann's constant,  $T$  is the absolute temperature,  $\Delta f$  is the noise bandwidth,  $g_m = \sqrt{2\beta J}$  in average when  $I_{in} < J$ , and  $\beta$  is the transconductance parameter. Only the thermal noise component, was considered. The relationship of  $\overline{V_{n1}^2} = \overline{V_{n2}^2} = \overline{V_n^2}$  and  $I_{out} = I_{in}$  is also assumed. Then, the S/N is calculated as

$$\begin{aligned} S/N &= 10 \times \log(I_{out}^2 / 2g_m^2 \overline{V_n^2}) \\ &= 10 \times \log\{I_{in}^2 / (16kT/3)(\sqrt{2\beta J})\Delta f\} \end{aligned} \quad (2)$$

Equation (2) indicates that the S/N greatly depends on the  $I_{in}$  value and that it degrades when the product  $\beta J$  becomes large. It also implies that  $I_{in}$  cannot be reduced by much and that there must be a power reduction limit. We decided to investigate whether this noise characteristic of a basic current mirror circuit appears in an actual current-mode circuit. To verify this, we designed and fabricated a current-mode sample-and-hold circuit, because it is one of the major analog functions frequently used in front of an analog-to-digital converter. Since a sample-and-hold circuit belongs to a sampled data system, the fold-over phenomenon of the noise appeared. This is also analyzed in this paper.

### 3. A Full Current-Mode Sample-and-Hold Circuit

The designed sample-and-hold circuit operates with a 20 MHz clock frequency from a 3 V power supply. The use of analog switches is necessary when it is implemented. An analog switch produces substantial feed-through error when it is turned off; therefore, this error source must be canceled to observe the noise performance. One way to accomplish this is to place analog switches at both inputs of a differential amplifier, as originally proposed in Ref. [6]; this is illustrated in Fig. 2. The feed-through error from the switches was applied equally to the inputs of the differential pair M1

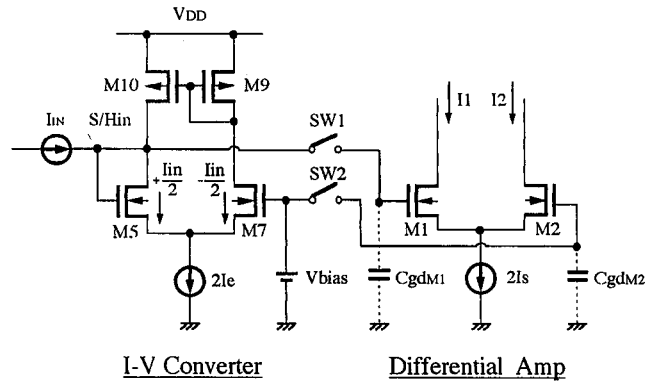


Fig. 2 A conceptual schematic of the sample-and-hold circuit.

and M2, and was suppressed by the common mode rejection characteristic of the differential amplifier. The output current was produced by taking the difference current  $I_1 - I_2$ .

A single-ended input signal was used in this design so that the input circuit would be simplified and there would be only one input terminal on the LSI chip. Since sample switches are differentially placed in the circuit, they need to be biased in the same DC voltage. Those DC voltages were produced in the  $I-V$  converter shown in Fig. 2. The  $I-V$  converter consisted of transistors M5, M7, M9, M10, and a constant current source  $2I_e$ . It had the configuration of a voltage buffer amplifier. Voltage at the S/H<sub>in</sub> terminal became equal to  $V_{bias}$  if the feedback gain (which is the gain of transistor M10) was large. The transconductance  $g_m$  and the output conductance  $g_{ds}$  of M10 were selected to  $412 \mu S$  and  $7 \mu S$ , with a bias current of  $180 \mu A$ . A cascode connection of transistors was used for all transistors in the  $I-V$  converter; therefore, the feedback gain became large to ensure the buffer operation. As a result, the DC voltages at the gates of M1 and M2 and the analog switches were equal. The  $V_{bias}$  was selected as  $V_{DD}/2$  so that a complementary MOS analog switch could be used. When the input current,  $I_{in}$ , was applied to the  $I-V$  converter (Fig. 2),  $+I_{in}/2$  and  $-I_{in}/2$  of the signal current flowed in M5 and M7. Although the voltage change across the gates of M5 and M7 was suppressed, there was still modulation of the switch resistance caused by the input signal change. This caused a change in the time constant formed by the switch's on-resistance and a hold capacitor (in this case,  $C_{gdM1}$  plus a  $0.3 pF$  of additionally connected capacitor). As a result, the frequency characteristic at the gate of M1 changed depending on the voltage level, producing a gain error. A complimentary MOS analog switch is considered to be best for achieving small on-resistance variation; however, selecting  $V_{bias}$  to  $V_{DD}/2$  may lead to larger on-resistance than in a different biasing scheme. In spite of this, the switch size should be minimized to suppress the unnecessary feed-through component. We used a transistor with a

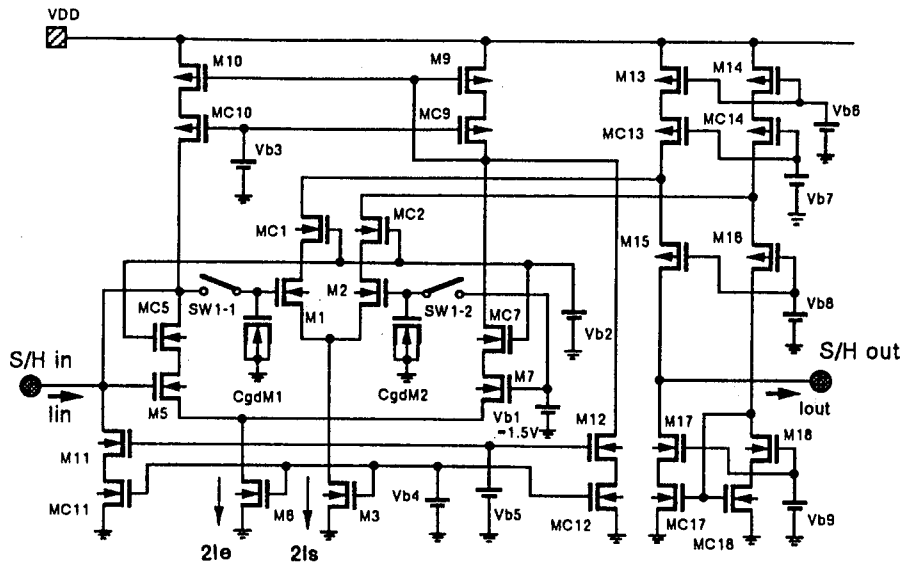


Fig. 3 The actual designed sample-and-hold circuit.

low threshold voltage ( $V_{th}$ ) for the analog switches to obtain a sufficiently low on-resistance for a 20 MHz operation with a small switch size. The designed value of the switch on-resistance was 2 k $\Omega$ . The  $V_{bias}$  of  $V_{DD}/2$  gave enough reverse bias voltage for the analog switches when they were turned off as well as the opportunity to use low  $V_{th}$  transistors without problems from leakage current. A precise transformation of the input current to the output of the differential amplifier was also necessary. The voltage produced across the gates of M5 and M7 became the input for the gates of M1 and M2; it was then converted back to current by the differential amplifier M1 and M2. When both switches, SW1 and SW2 in Fig. 2, were on, the output current  $I_{out}$  became

$$\begin{aligned}
 I_{out} &= I_1 - I_2 \\
 &= I_{in} \\
 &\times \sqrt{1 + (4/I_{in}^2)(I_s - I_e) \times \{2I_e - \sqrt{(2I_e)^2 - I_{in}^2}\}}
 \end{aligned}
 \tag{3}$$

when  $I_s = I_e$ ,  $I_{out}$  became equal to  $I_{in}$ .

In this design, transistors M1, M2, M5 and M7 were 60  $\mu\text{m}/1.35 \mu\text{m}$  ( $W/L$ ) in size, M9 and M10 were 45  $\mu\text{m}/2.45 \mu\text{m}$ , and the switch sizes of SW1 and SW2 were 3.8  $\mu\text{m}/0.6 \mu\text{m}$ . Figure 3 shows the actual designed circuit. Since the voltage change at various nodes caused by the input signal change affected the precise current transformation, a cascode connection of transistors was used throughout the circuit. The circuit in Fig. 3 also had the output circuit where the difference current  $I_1 - I_2$  was produced as an single-ended output current at the S/H<sub>out</sub> terminal.

#### 4. Experimental Results

A photograph of the fabricated chip is shown in Fig. 4.

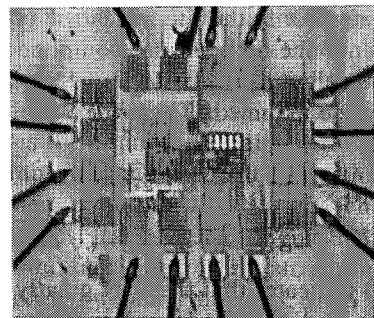


Fig. 4 Photograph of the sample-and-hold chip.

The chip successfully operated with a 20 MHz clock from 3 V power supply [7]. Figure 5 shows the measurement setup. An input signal generator was synchronized with a clock generator. The signal and bias currents for the input circuit on the chip were supplied by external resistors. The output current of the sample-and-hold circuit, which was changed to a single-ended current internally, was converted back to voltage by an external operational amplifier. The -3 dB bandwidth of this current to voltage converter was 10 MHz. A two-stage emitter follower interfaced with a measuring instrument, such as a spectrum analyzer. Figures 6 and 7 show the measured input frequency versus the S/N characteristics for the 3 V and 5 V supply voltages. Both sample-mode and sample-and-hold mode S/Ns are plotted in the figures. The clock speed was 20 MHz and the noise bandwidth was 10 MHz. Input currents of  $\pm 115 \mu\text{A}$  and  $\pm 220 \mu\text{A}$  were the maximum for the 3 V and 5 V power supplies, and the S/N measurement was done with these current values and supply voltages. For the input current of  $\pm 115 \mu\text{A}$ , 57 dB of the sample-mode S/N and 51 dB of the sample-and-hold mode S/N were obtained up to a

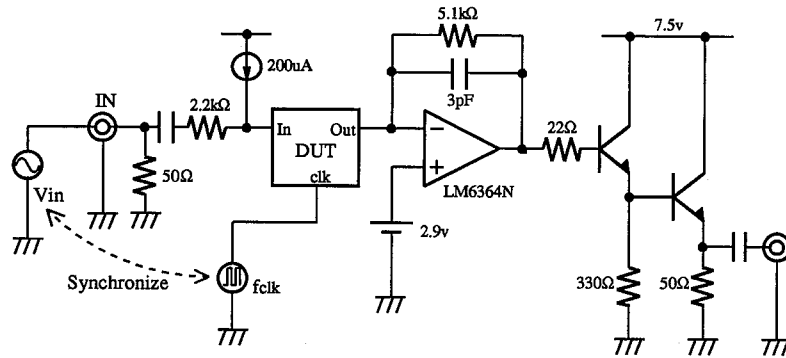


Fig. 5 The test setup of the sample-and-hold circuit.

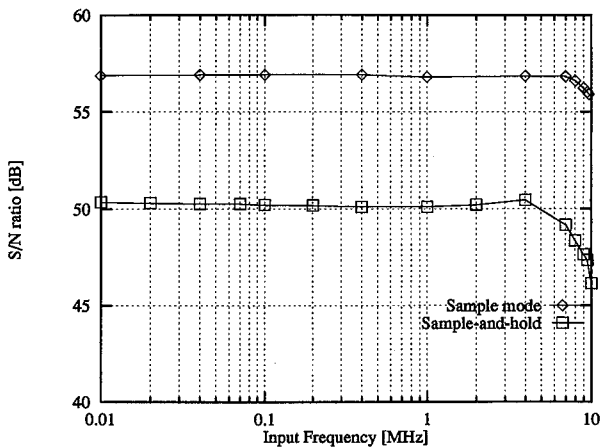


Fig. 6 Input frequency versus S/N ratio ( $V_{DD} = 3\text{ V}$ ,  $I_{in} = \pm 115\ \mu\text{A}$ ,  $2I_e = 180\ \mu\text{A}$ ).

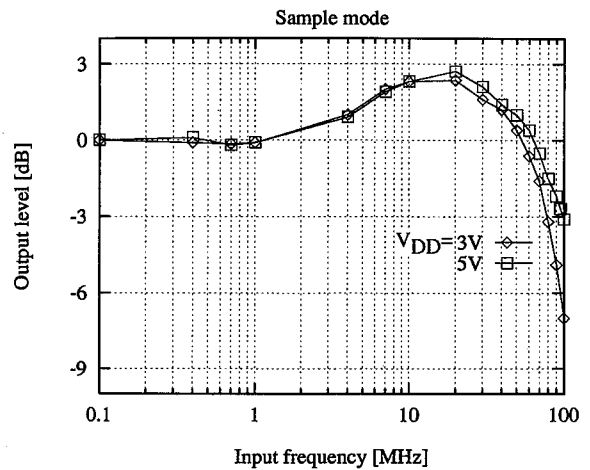


Fig. 8 Overall input to output frequency characteristics in sample mode (Input level =  $-10\ \text{dB}$  of F/S).

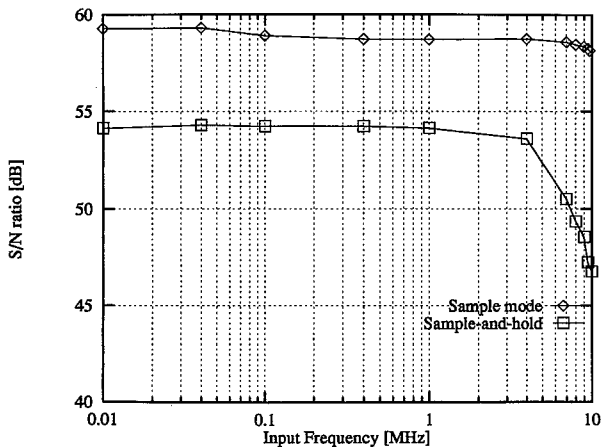


Fig. 7 Input frequency versus S/N ratio ( $V_{DD} = 5\text{ V}$ ,  $I_{in} = \pm 220\ \mu\text{A}$ ,  $2I_e = 300\ \mu\text{A}$ ).

5 MHz input signal. The sample-and-hold mode S/N degraded to 47 dB as the input signal frequency was increased to 10 MHz. With an input current of  $\pm 220\ \mu\text{A}$ , the sample-mode and sample-and-hold mode S/Ns became 59 dB and 54 dB. Figure 8 shows the frequency versus voltage gain characteristic of the overall sample-and-

hold amplifier, including the input and output circuits when in sample mode. There was no significant difference between the 3 V and 5 V power supplies. About 2.5 dB of peak can be seen at 20 MHz. The gain of a sample-and-hold circuit in Fig. 3 decreased at a high frequency, due to the time constant formed with the switch on-resistance and the hold capacitor; the input circuit was designed to compensate for this by applying a positive feedback to increase the gain at high frequencies. Figure 8 shows that the amount of the positive feedback was larger and the selected peak frequency was smaller than our expected values. The overall  $-3\ \text{dB}$  bandwidth became 80–100 MHz. Figure 9 shows the S/N dependency on the duty ratio  $\tau_{sh}$ .  $\tau_{sh}$  is the hold interval normalized by the clock interval. When  $\tau_{sh}$  became small, the S/N approached the value in the sample mode. Figure 10 shows the results of measuring the S/N dependency on the input current by varying the bias current  $2I_e (= 2I_s)$  in Fig. 3. A higher S/N value was obtained with a low bias current when the input current was the same.

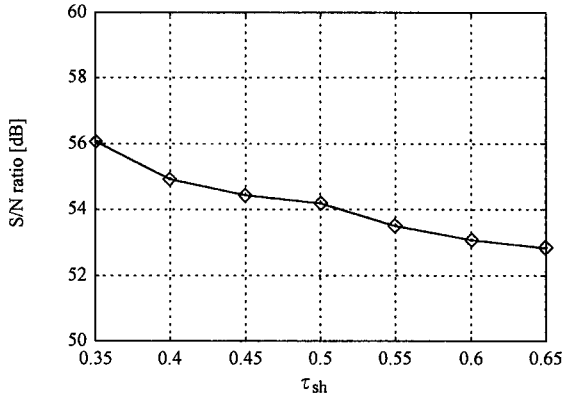


Fig. 9 Hold-time duty ratio versus S/N in sample-and-hold mode ( $f_{in} = 1$  MHz,  $V_{DD} = 3$  V).

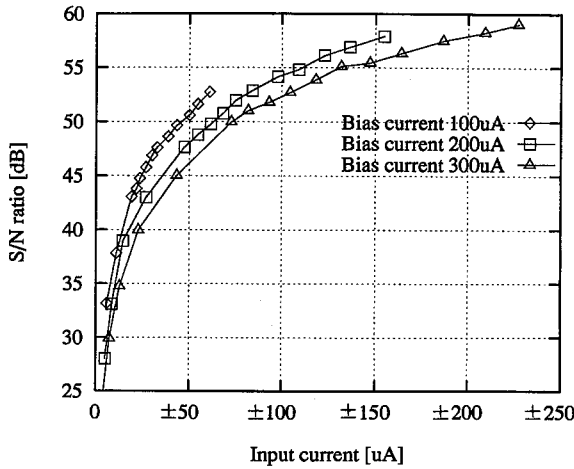


Fig. 10 S/N ratio versus input current characteristic with different bias currents in sample mode ( $f_{in} = 1$  MHz,  $V_{DD} = 5$  V).

## 5. Noise Analysis

### 5.1 S/N Difference between Sample Mode and Sample-and-Hold Mode

We analyzed the fold-over phenomenon of the noise occurred in this sample-and-hold-circuit. The S/N degradation in the sample-and-hold mode, based on the S/N in the sample mode, was analyzed in Ref. [8], which states that the output noise spectrum density  $\eta_{out}(f)$  of a sample-and-hold circuit becomes

$$\eta_{out}(f) \leq \eta_n [2\tau_{sh}^2 (BW_n/f_s) \text{sinc}^2(\tau_{sh}f/f_s) + 1 - \tau_{sh}] \quad (4)$$

under  $BW_n \geq 10 f_s$  conditions, where  $\eta_n$  is the uniform noise spectrum density of the input noise source,  $BW_n$  is the equivalent noise bandwidth,  $\tau_{sh}$  is the duty ratio,  $\text{sinc}(x) = \sin(x)/x$  and  $f_s$  is the sampling frequency.  $BW_n$  becomes

$$BW_n = 1/4CR_{on} \quad (5)$$

where  $C$  is the total capacitance, which is composed of an additional connected 0.3 pF capacitor at the gate of transistor M1 or M2 plus the input capacitance  $C_{gdM}$  (Fig. 2), and  $R_{on}$  is the switch on-resistance. In this design,  $C$  and  $R_{on}$  were estimated to be approximately 0.6 pF and 2 k $\Omega$  from the circuit simulation. This yielded a  $BW_n$  of approximately 200 MHz. Taking the duty  $\tau_{sh}$  as 0.5 and  $f_s = 20$  MHz, and further assuming that the sinc function was close to 1 in the range of  $f < 10$  MHz, we obtained the ratio of  $\eta_{out}$  to  $\eta_n$  in the observed range to be 5.5. Taking the power of this ratio yielded the difference in S/N between the sample mode and sample-and-hold mode, which was calculated to be 7.4 dB. The data given in Fig. 6 agrees well with this result, although that in Fig. 7 is slightly smaller. Equation (4) indicates that when  $\tau_{sh}$  becomes small,  $\eta_{out}(f)$  becomes small, and therefore the S/N is improved. Figure 9 verifies this. To improve the S/N, the time constant  $CR_{on}$  must be maximized. However,  $R_{on}$  can not be increased because it generates thermal noise. Thus, we should increase the value of  $C$ .

### 5.2 S/N Dependency on Bias and Input Currents

Next, we analyzed the S/N difference between those given in Figs. 6 and 7. There was 4 dB difference between the sample-and-hold mode S/Ns. The major differences in those circuits were the input current  $I_{in}$  and the bias current  $2I_e$ . When an input current  $I_{in1}$  was applied to the  $I$ - $V$  converter shown in Fig. 2, a current change of  $+I_{in1}/2$  occurred in transistor M5. If the transconductance and the gate-to-source voltage change of M5 are  $g_{m1}$  and  $\Delta V_g$ , then

$$g_{m1} \times \Delta V_g = I_{in1}/2 \quad (6)$$

Since a current change of  $-I_{in1}/2$  occurred in M7, a voltage change of  $\Delta V_1$  was produced across the gates of M5 and M7. This voltage change was applied to the gates of M1 and M2 of a differential pair and it became

$$\Delta V_1 = 2 \times \Delta V_g = I_{in1}/g_{m1} = I_{in1}/\sqrt{2\beta I_{e1}} \quad (7)$$

where  $I_{e1}$  is half of the tail bias current. Similarly, the voltage change of  $\Delta V_2$  across the gates of M1 and M2, when the input current and bias current changed to  $I_{in2}$  and  $I_{e2}$ , was calculated as follows:

$$\Delta V_2 = I_{in2}/\sqrt{2\beta I_{e2}} \quad (8)$$

However, the device noise was inversely proportional to  $\sqrt{2\beta I_e}$  from the discussion in Sect. 2. The noise from the switch on-resistance did not change with the bias current change because the voltage applied to the switch did not change. If we neglect the influence of the noise from the switch on-resistance on the total noise power, then

$$\overline{V_n^2} \propto 1/\sqrt{2\beta I_e} \quad (9)$$

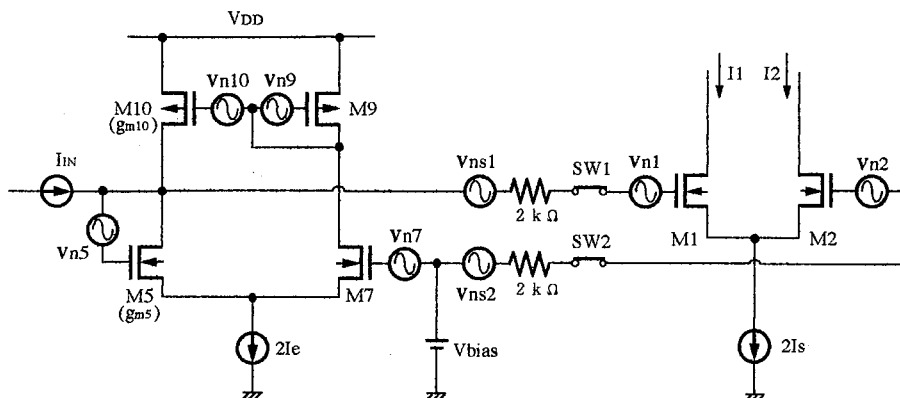


Fig. 11 Dominant noise sources in a sample-and-hold circuit.

The S/N difference for these two cases ( $\Delta S/N$ ) yields

$$\begin{aligned} \Delta S/N &= 10 \log\{(\Delta V_2)^2 \overline{V_{n1}^2} / (\Delta V_1)^2 \overline{V_{n2}^2}\} \\ &= 10 \log[(I_{in2}/I_{in1})^2 (I_{e1}/I_{e2})^{1/2}] \end{aligned} \quad (10)$$

Substituting the values of  $I_{in1} = 115 \mu\text{A}$  and  $2I_{e1} = 180 \mu\text{A}$  in Fig. 6 and  $I_{in2} = 220 \mu\text{A}$  and  $2I_{e1} = 300 \mu\text{A}$  in Fig. 7, the  $\Delta S/N$  becomes 4.5 dB. This is consistent with the measured data. The measurements of the S/N dependency on the various input currents and the three different bias currents in the sample mode are given in Fig. 10. In this case, the S/Ns were measured with a 5 V supply voltage because  $220 \mu\text{A}$  of input current cannot be applied when a 3 V supply voltage was used. The bias current could be chosen independently of the supply voltage and this setup does not affect the discussion. The graph displays three different curves for the bias currents of  $100 \mu\text{A}$ ,  $200 \mu\text{A}$ , and  $300 \mu\text{A}$ . The calculated value of  $\Delta S/N$  with  $50 \mu\text{A}$  of input current, with a bias current difference of  $100 \mu\text{A}$  and  $200 \mu\text{A}$ , and of  $100 \mu\text{A}$  and  $300 \mu\text{A}$ , became  $-1.5 \text{ dB}$  and  $-2.5 \text{ dB}$ , while the measured data became  $-2.5 \text{ dB}$  and  $-4 \text{ dB}$ . Square-root dependence of the  $\Delta S/N$  on the bias current can be seen in the figure, however, there is still a little difference between the calculation and measured data. If the input current was doubled, the S/N would be expected to increase 6 dB from Eq. (10). The S/N difference between the input current of  $50 \mu\text{A}$  and  $100 \mu\text{A}$  was measured 6 dB and 6.5 dB for the bias current of  $200 \mu\text{A}$  and  $300 \mu\text{A}$ . The data in Fig. 10 coincides with this calculation.

These factors demonstrate that the S/N of the circuit in Fig. 3 was greatly affected by the input current and bias current values. Moreover, the S/N value was proportional to the square of input current and is nearly proportional to the square-root of the bias current. This fact agrees well with the discussion in Sect. 2.

### 5.3 S/N Estimation Based on Device Noise Sources

The S/N value in the sample mode had not been detected yet. We attempted to calculate the S/N value

based on the noise sources which are incorporated with various devices in the circuit. Figure 11 shows the circuit with those noise sources. In this case, noise sources from cascode transistors are not considered although actual circuit has many cascode transistors as shown in Fig. 3. This is because the AC gain of a cascode transistor is very low and its noise does not appear at the output. This point was confirmed by the SPICE noise analysis in advance. In Fig. 11, noise sources of the switches' on-resistances are represented as  $V_{ns1}$  and  $V_{ns2}$ . The transistor generated noise, which originated from the channel resistance and is represented in the figure as  $V_n$ . In this case, the total noise power,  $\overline{V_{ntotal}^2}$ , which appeared at the gates of M1 and M2, was calculated by assuming that either  $V_{ns1}$  or  $V_{ns2}$  was the thermal noise generated by the switches' on-resistance  $R_{on}$ . The transistor's noise ( $V_n$ ) was also a thermal noise related to channel resistance and is expressed in terms of  $g_m$  [9]; i.e.,

$$\begin{aligned} \overline{V_{nsx}^2} &= 4kTR_{on}\Delta f \\ \overline{V_{ny}^2} &= (8kT/3g_{my})\Delta f \end{aligned} \quad (11)$$

where  $k$  is the Boltzmann's constant;  $T$  is the absolute temperature;  $\Delta f$  is the noise bandwidth;  $x$  is 1 or 2; and  $y$  is 1, 2, 5, 7, 9 or 10.

$V_{n5}$  and  $V_{n7}$  appeared at the gate of M1 because the gain of the  $I$ - $V$  converter circuit was 1.  $V_{n9}$ , and  $V_{n10}$  appeared at the gate of M1 with a gain of  $2g_{m10}/g_{m5}$ , where  $g_{m10}$  and  $g_{m5}$  are transconductances of transistors M10 and M5.  $V_{ns1}$  and  $V_{n1}$  appeared at the gate of M1, and  $V_{ns2}$  and  $V_{n2}$  appeared at the gate of M2, with a gain of 1. The total noise power,  $\overline{V_{ntotal}^2}$ , therefore, became,

$$\begin{aligned} \overline{V_{ntotal}^2} &= \overline{V_{n5}^2} + \overline{V_{n7}^2} \\ &\quad + (2g_{m10}/g_{m5})^2 (\overline{V_{n9}^2} + \overline{V_{n10}^2}) \\ &\quad + \overline{V_{ns1}^2} + \overline{V_{n1}^2} + \overline{V_{ns2}^2} + \overline{V_{n2}^2} \end{aligned} \quad (12)$$

However, the signal voltage  $\Delta V$ , which was applied to the gate of M1, was  $I_{in}/g_{m5}$ , as discussed in Eq. (6), and the rms signal power became

$$(\Delta V_{rms})^2 = (I_{in\ rms}/g_{m5})^2 \quad (13)$$

The S/N ratio is calculated as

$$S/N = 10 \log(\Delta V_{rms})^2 / \overline{V_{ntotal}^2} \quad (14)$$

Using the measuring conditions in Fig. 6, these values become

$$\begin{aligned} g_{m5} &= 9.15E - 04, g_{m10} = 4.12E - 04, \\ \overline{V_{n1}^2} &= \overline{V_{n2}^2} = \overline{V_{n5}^2} = \overline{V_{n7}^2} = 1.24E - 10, \\ \overline{V_{n9}^2} &= \overline{V_{n10}^2} = 2.76E - 10, \\ \overline{V_{ns1}^2} &= \overline{V_{ns2}^2} = 3.31E - 10, \end{aligned}$$

and

$$\Delta V_{rms} = 88.9 mV_{rms}.$$

The switches' on-resistance was  $2k\Omega$  and  $\Delta f = 10$  MHz. Substituting these into Eq. (14) yields a S/N ratio of 66.9 dB.

This calculated S/N value is 9-10 dB larger than that from the measured data given in Fig. 6. Considering the example calculation above, we concluded that the device noise largely influences the overall noise performance. Since the actual sample-and-hold test chip accommodated the bias, input and output circuits interfacing with the outside of the chip, and the voltage gain from each of input and output circuit was set nearly equal to 1, as can be seen in Fig. 8, we believe that the device noises in those circuits were also added to the noise in Eq. (12). The SPICE noise analysis also indicated this. Therefore, the total noise power could easily be doubled or tripled. For reasons not presently clear, there was still a 4-7 dB difference between the measured data and the calculation, but the calculation clearly indicates that the S/N limit exists around 60-65 dB in the sample mode under the measurement conditions shown in Fig. 6. The low S/N value was mainly due to the suppressed voltage amplitude at the output of the  $I$ - $V$  converter. Since the circuit shown in Fig. 2 is a differential realization based only on a basic current mirror circuit, this result implies a serious constraint to current-mode analog circuits, because a voltage change from the input signal is always suppressed in those circuits. The input current value can be increased to avoid a poor S/N ratio, but this then leads to increases in the circuit current and power consumption.

## 6. Conclusion

We studied the S/N characteristics of a sample-and-hold amplifier with a full current-mode approach through the design, circuit simulation, and chip evaluation to investigate the potential application of an MOS current-mode analog circuit for future LSIs. The S/N limiting factors were analyzed in a simple current mirror circuit. In order to verify this, the S/N characteristics of a full current-mode 3 V, 20 MHz sample-and-hold circuit was

measured. Through extensive noise analysis and measurement, we found that the current-mode circuit was sensitive to device noises, because the signal voltages at the intermediate nodes in a circuit were always suppressed. Moreover, we found that its S/N depends the square of the input current value and the nearly square-root of the bias current value. This fact poses a serious problem to future LSIs because the input current cannot be decreased, and therefore the power cannot be reduced when a current-mode approach is used to achieve a high-precision, low-voltage, high-speed operation of an analog circuit. Since signal voltage suppression is the main feature of a current-mode circuit, there must be a trade-off between low-power and low-voltage operation and high-precision performance.

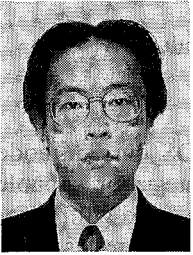
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