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Study of a Low Voltage, Low Power and High Frequency CMOS VCO Circuit

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SUMMARY This paper examines the feasibility of a high frequency (more than 1 GHz) ring-oscillator-type CMOS VCO, able to maintain a good linearity between the oscillator output frequency and control voltage, while preserving low voltage and low power operation capabilities. A CMOS VCO circuit, with a newly developed current-controlled delay cell and an architecture combining the transitions of each delay cell output, with high-frequency operation, was designed and simulated using the CMOS 0.6 μm device parameters. We analyzed the generation of unnecessary harmonics and sub-harmonics when a delay cell's propagation delay time varied. The simulation indicated that a CMOS VCO with a frequency range of 200 MHz to 1.4 GHz, a power dissipation of 8.5 mW at 900 MHz from a 3 V power supply, and an operation voltage of 1 V to 3 V can be implemented on a chip.

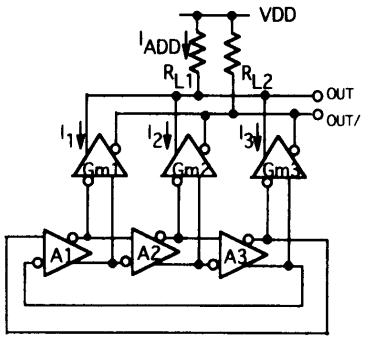
key words: *CMOS VCO circuit, high frequency VCO, current-controlled differential delay cell, combined signal output*

1. Introduction

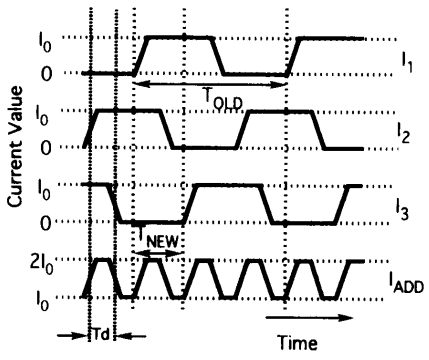
High frequency VCOs are widely used in communication equipment and microprocessors [1], [2]. Ring-oscillator-type VCOs have been studied intensively because they are easily constructed using standard CMOS circuits. However, the high-frequency operation of ring-oscillator-type VCOs is difficult, and there is poor linearity between the output frequency and the control voltage. The linearity has been improved [3], [4]. In addition, a new architecture combining the transitions at each output of a delay cell in a ring oscillator has been proposed for high frequency operation [5]. However, it has only been demonstrated in bipolar VCO circuits, and it is not clear whether it is applicable to CMOS VCO circuits. Low power and low voltage operation capabilities are required even for high-frequency VCOs [6]. We studied ring-oscillator-type CMOS VCO circuits to determine whether high frequency, low power and low voltage characteristics could be observed. The circuit was designed and simulated using CMOS 0.6 μm device parameters.

2. Analysis of a New VCO Architecture

The idea for the VCO configuration described in this paper is based on that in [2]. Figure 1(a) shows a block diagram of a VCO consisting of three differential delay cells (A1, A2, and A3) connected in series, and three Gm cells (Gm1, Gm2, and Gm3). The Gm cell converts the voltage change at the output of each delay cell into a current. The current output of a Gm cell switches from 0 to a constant value of I_0. The current output of each Gm cell is combined into one and applied to load resistors R_{L1} and R_{L2}. The sum of currents I_1, I_2 and I_3 becomes I_{ADD}, which flows through R_{L1} (Fig. 1(a)). Waveforms of I_1, I_2, I_3 and I_{ADD} are shown in Fig. 1(b). The waveform of I_2, corresponding to the voltage change at the output of A2, is the inverted and delayed version of I_1. Similarly, the waveform of I_3 is the inverted and delayed version of I_2. The propagation delay time of a delay cell is Td. With I_{ADD} as the sum of I_1, I_2 and I_3, its value changes from



(a) Block diagram of a VCO.



(b) Waveforms of currents I_1, I_2, I_3, and I_{ADD}.

Fig. 1 A VCO circuit and waveforms of various currents in the circuit.

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I_0 to $2I_0$ (or $2I_0$ to I_0) in synchronizing with each transition of I_1, I_2, and I_3. Thus the output frequency at terminal OUT becomes triple that of a ring oscillator. Corresponding output is at terminal OUT/.

This configuration generates unnecessary spectral components due to the mismatched propagation delay time among delay cells. The VCO output waveform during a mismatch is shown in Fig. 2. We assumed that the propagation delay time of only one delay cell out of three changed from τ to $\tau-\Delta$. Taking the Fourier transform of the waveform in Fig. 2 yields:

$$f(t)=\sum_{-\infty}^{\infty}(j/n\pi)[1-\cos n\pi-2\cos(2n\pi\tau/T)+\cos\{2n\pi(2\tau-\Delta)/T\}]e^{j2n\pi t/T} \quad (1)$$

Calculating coefficients up to 20th of n in Eq. (1) generates the power spectrum shown in Fig. 3. Three different cases of Δ varying 1%, 2%, and 5% of the time interval τ were analyzed. The results are given in Fig. 3. The 3rd harmonic component was the desired output. When no mismatch occurred, only 3rd, 9th, 15th, etc. components appeared, while the unnecessary frequency components, such as 1st, 5th, 7th, etc. appeared, if Δ is not zero. The power levels of the unnecessary components were -44 dB, -38 dB and -30 dB below that of a desired output when Δ is 1%, 2% and 5% of τ, respectively. The 5% change corresponds to the 25 pS of time change when the output frequency is 1 GHz. Unnecessary components with a power level of -30 dB may be tolerable, although further study is necessary. In reality, the shape of the output is close to sinusoidal in high frequency, and so the criteria can be broadened somewhat from that used in this ideal situation.

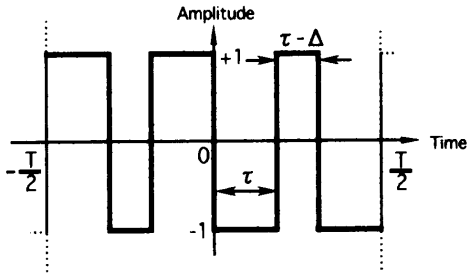


Fig. 2 VCO output waveform with a mismatched delay.

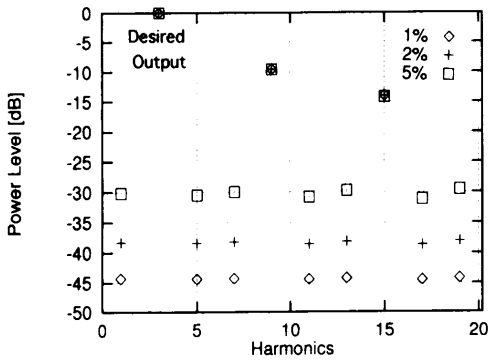


Fig. 3 Power spectrum of VCO output with a mismatched delay.

3. VCO Circuit Design

The designed and simulated VCO block diagram is shown in Fig. 4. A ring oscillator was composed of five stages of delay cells. The combined currents I_{L1} and I_{L2} of five Gm cells were fed to loads MPG1 and MPG2, which were diode connected PMOS transistors. Each stage consisted of two current-controlled differential delay cells connected in a series. This is because the signal level of a combined output decreases due to the overlapping transitions which occur when the current in a delay cell increases and the propagation delay time shortens. Figure 5(a) shows the circuit of a delay cell and Fig. 5(b) shows the circuit of a Gm

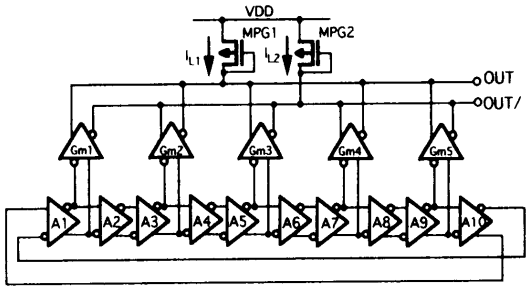
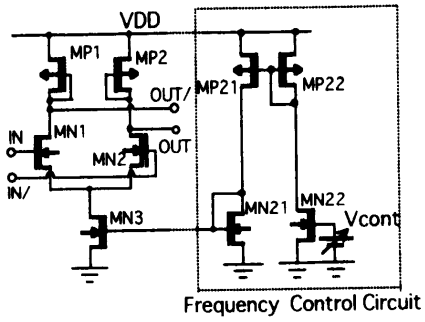
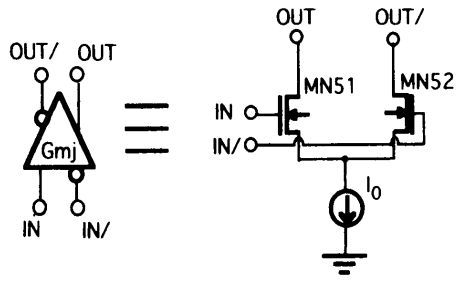


Fig. 4 Block diagram of the designed and simulated VCO circuit.



(a) Delay cell circuit.



(b) Gm cell circuit.

Fig. 5 VCO cell circuits.

cell. The delay cell consists of a differential amplifier with input transistors MN1 and MN2, and the diode connected transistors MP1 and MP2 as loads. We controlled the delay by changing the current flowing through MN3. The current value flowing through MN3 was proportional to the square of the control voltage V_{cont}, and the relationship between the VCO frequency and the control voltage became linear [1]. The frequency control circuit which produced the control current is shown in Fig. 5(a) in the box bordered with a dotted line. A Gm cell consists of a differential amplifier with a fixed bias current of I_0 as shown in Fig. 5(b). The output current of a Gm cell switches from 0 to I_0 when synchronizing with transitions at the output of a delay cell. I_{L1} and I_{L2} in Fig. 4 become the sum of the currents from five Gm cells, their current value changing between $2I_0$ and $3I_0$. Next we calculated the minimum supply voltage of a delay cell. The highest voltage level at one of the gates of transistors MN1 and MN2 of the delay cell in Fig. 5(a) was $VDD-V_{th}$, where V_{th} is the threshold voltage of the transistor. When the terminal IN becomes high, the current I flowing through MN3 flowed through MP1 and MN1. The gate-to-source voltage of MN1 becomes $\sqrt{(2I/\beta_{MN1})}+V_{th}$, where $\beta=\mu_n C_{ox}W/L$. If MN3 operated in the saturation region, the allowable minimum drain-to-source voltage was $\sqrt{(2I/\beta_{MN3})}$. In this condition, the minimum voltage supply became:

$$VDD_{\min}=2V_{th}+2\sqrt{(2I/\beta)} \tag{2}$$

where βs of MN1 and MN3 were assumed equal. $\sqrt{(2I/\beta)}$ is commonly a few hundred millivolts and $VDD_{\min}$ becomes very low.

4. Simulation Result

To verify that the VCO circuit in Fig. 4 had low voltage, low power and high frequency capabilities, it was computer simulated by the SPICE circuit simulation program. We used the 0.6μm CMOS process device parameters. The threshold voltage was +0.2 V (−0.2 V) for NMOS (PMOS). The solid line in Fig. 6 shows the oscillation frequency versus the control voltage ($V_{cont}-V_{th}$) characteristic. The supply voltage was 3 V and ($V_{cont}-V_{th}$) changed from 0.2 V to 2.8 V. The linear relationship between the oscillation frequency and the control voltage was verified, as was operation above 1 GHz. The dotted line is the characteristic of a 10-stage ring oscillator without the combined output, using current-controlled differential delay cells. The oscillation frequency of a VCO with a combined output is five times greater than that of a conventional ring-oscillator-type VCO.

Figure 7 shows the waveforms of a VCO with a 1 V power supply. The voltage change at each output of A1, A3, A5, A7 and A9, and between terminals OUT and OUT/(V_{out}), is shown. The maximum of ($V_{cont}-V_{th}$) is only 0.8 V, and the output frequency is 500 MHz. Although the voltage level at the combined output was lower than expected, the results in Fig. 7 show definite low voltage operation. With more control voltage, even with a 1 V power supply, an oscillation frequency near 1 GHz is expected. Discovering the means to boost the control voltage is a goal for further study. Table 1 summarizes the overall performance of the VCO circuit. When $VDD=3$ V, the power consumption was 8.5 mW with $V_{cont}=1.5$ V, at 900 MHz oscillation. The oscillation frequency ranged from 200 MHz to 1.4 GHz as the V_{cont} changed from 0.4 V to 3 V.

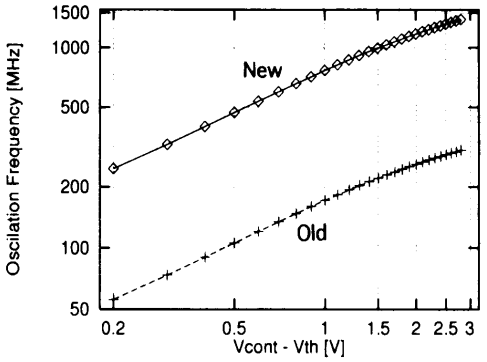


Fig. 6 Oscillation frequency vs. control voltage characteristics.

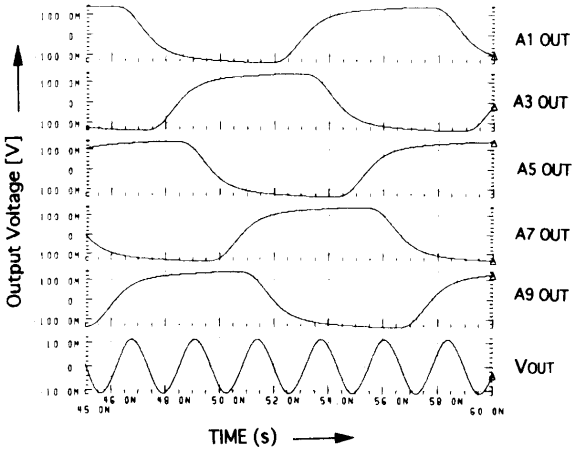


Fig. 7 Waveforms of the circuit in Fig. 4 with a 1 V power supply.

Table 1 Overall performance of the VCO circuit.

Items	Value	Unit
Supply voltage	1~3	V
Oscilation frequency Range (V_{DD}=3V)	200~1400	MHz
Power dissipation (V_{cont}=1.5V, V_{DD}=3V)	8.5	mW
Threshold voltage PMOS NMOS	−0.2 +0.2	V
Process	0.6μm CMOS	

5. Conclusion

A CMOS VCO circuit was designed and simulated; it oscillated above 1 GHz and had low power and low voltage characteristics. We used a current-controlled differential delay cell for the delay cells in a ring oscillator, and adopted an architecture which combined the transitions at the output of each stage of delay cells. The simulation results show low voltage operation(1 V), power dissipation of 8.5 mW with a 3 V supply when the oscillation frequency was 900 MHz (low power), and an oscillation range of 200 MHz to 1.4 GHz with a 3 V supply(high frequency). We studied the unnecessary generation of harmonics and sub-harmonics caused by mismatched delays in delay cells. We believe this study should be continued, as should the development of a technique to boost the control voltage of a VCO operating with a low supply voltage, and the output circuit design.

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